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A Review on Enhancement of SRAM Memory Cell

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ABSTRACT- *In this field research paper explores the design and analysis of Static Random Access Memory (SRAMs) that focuses on optimizing delay and power. CMOS SRAM cell consumes very little power and has less read and write time. Higher cell ratios will decrease the read and write time and improve stability. PMOS semiconductor unit with fewer dimensions reduces the ability consumption. During this paper, 6T SRAM cell is implemented with reduced power and performance is good according to read and write time, delay and power consumption. It's been noticed typically that increased memory capability will increase the bit-line parasitic capacitance that successively slows down voltage sensing, to avoid this drawback use optimized scaling techniques and more, get improve performance of the design. Memories are a core part of most of the electronic systems. Performance in terms of speed and power dissipation is the major area of concern in today's memory technology. During this paper SRAM cells supported 6T, 9T, and 8T configurations are compared based on performance for reading and write operations. During this paper completely different static random access memory is designed to satisfy low power, high-performance circuit and also the extensive survey on options of various static random access memory (SRAM) designs were reported. Improve performance static random access memory based on designing a low power SRAM cell structure with optimum write access power.*

Keywords: SRAM, Delay Power, Transistors, T6, DRAM

I. INTRODUCTION

Random-access memory (RAM) is a form of pc data storage that stores frequently used program instructions to extend the final speed of a system. A random-access device permits knowledge things to be read or written in nearly the same quantity of your time irrespective of the physical location of information within the memory. In contrast, with different direct-access data storage media comparable to hard disks, CD-RWs, DVD-RWs and also the older drum memory, the time needed to read and write knowledge things varies considerably depending on their physical locations on the recording medium, because of mechanical limitations such as media rotation speeds and arm movement Static Random Access Memory (SRAM) is scan/write memory devices which will read data from or write data to any of its memory addresses. The requirement for low power integrated circuits is well known due to their extensive use within the electronic portable equipments. On-chip SRAMs (Static Random Access Memory) confirm the power dissipation of SoCs (System on Chips) additionally to its speed of operation. Therefore it is important to own energy economical SRAMs. The use of SRAM is expected to extend in the future for each portable and high-performance microchip. SRAM plays a crucial role in the modern microchip system, portable devices like PDA, cellular phones, and transportable multimedia system devices. To achieve a higher speed microchip, SRAM primarily based cache memories are ordinarily used. The trend of scaling of the device brings many challenges like power dissipation, sub-threshold run, reverse diode run, and stability [1]. These days analysis of terribly low threshold voltage and ultra-thin gate chemical compounds are in the progressive stage, thanks to reduction within the threshold voltage and also the gate oxide thickness. The phenomena like intrinsic parameter fluctuation, random do pant fluctuation, oxides thickness fluctuation, and line edge roughness more degrades the stability of SRAM cells. Giant scale integration and fabrication process have resulted in increased density of devices by decreasing the device physical dimensions. Performance in terms of low power dissipation and high-speed operation are the most important challenges of computer circuit style in deep submicron and nanoscale technologies. Designing a high-performance VLSI chip is becoming a necessity for mobile communication and computing devices. Advances in battery technology haven't taken place as quickly as advances within the electronic devices and systems. So, designing electronic systems having high performance in terms of high speed and low power dissipation may be a difficult task [2].

1.1 Types of Ram

I. Static RAM: SRAM may be a style of semiconductor memory that uses bistable latching circuitry to store every bit. The term static RAM differentiates it from dynamic RAM that should be periodically refreshed. Static RAM exhibits data remanence however it's still volatile within the standard sense that knowledge is eventually lost once the memory isn't powered.

II. Dynamic RAM: DRAM stores a small amount of data using a semiconductor device and capacitor combine, that along comprises a Dynamic RAM cell. The condenser holds a high/low charge, and the semiconductor device acts as a switch that lets the control circuitry on the chip read the capacitor's state of charge or changes it. This manner of memory is a smaller amount expensive to provide than static RAM; eventually, it's the predominant type of memory device utilized in modern computers. Dynamic RAM is thought of volatile because it lost |the information or data once power is off from the system [3].

1.2 Design of SRAM

A typical SRAM cell is created from six MOSFETs. Every bit in an SRAM is holding on four transistors (M1, M2, M3, and M4) that kind two cross-coupled inverters. This secondary cell has 2 stable states that are wont to denote zero and one. Two extra access transistors serve to manage access to a secondary cell throughout reading and write operations. Additionally, to such six-transistor (6T) SRAM, different kinds of SRAM chips use four, 8, 10 (4T, 8T, 10T SRAM), or a lot of transistors per bit. Four-transistor SRAM is sort of common in complete SRAM devices (as critical SRAM used for CPU caches), implemented in special processes with an additional layer of polysilicon, allowing for very high-resistance pull-up resistors. The principal disadvantage of using 4T SRAM is increased static power because of the constant current flow through one in all the pull-down transistors. Access to the cell is enabled by the word line that controls the two access transistors M5 and M6 that, in turn, control whether or not the cell ought to be connected to the bit lines: BL and complementary BL. they're wont to transfer data for each scan and write operations. Though it's not strictly necessary to possess two-bit lines, each the signal and its inverse are usually provided to enhance noise margins. Throughout read accesses, the bit lines are actively driven high and low by the inverters within the SRAM cell. The symmetric structure of SRAMs additionally permits for differential signaling, which makes little voltage swings a lot of simply detectable [4].

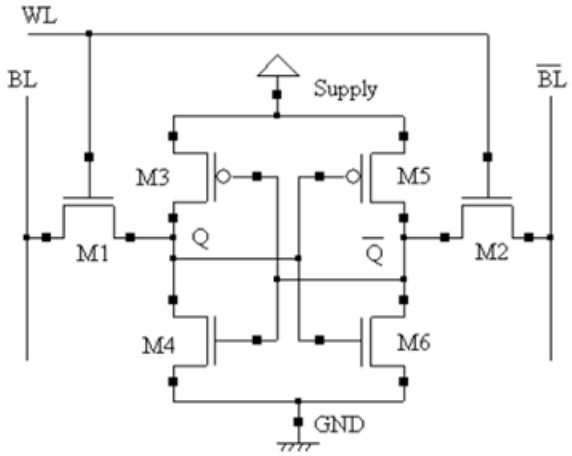

Figure 1: Design approach of SRAM

1.3 SRAM Memory Cell Operation

AN SRAM cell has three completely different states

1. Standby (the circuit is idle)
2. Reading (the data has been requested)
3. Writing (updating the contents)

1. **Standby**: If the word line isn't declared, the access transistors M5 and M6 disconnect the cell from the bit lines. The 2 cross-coupled inverters shaped by M1 – M4 can still reinforce one another as long as they're connected to the supply [5].

2. **Reading:**: In theory, reading only needs asserting the word line WL and reading the SRAM cell state by one access semiconductor and a bit line, e.g. M6, BL. however, bit lines are comparatively long and have massive parasitic capacitance. to speed up reading, an additional advanced method is used in practice: The browse cycle is started by recharging each bit lines BL and BL, i.e., driving the bit lines to a threshold voltage (midrange voltage between logical one and 0) by an external module (not shown within the figures). Then asserting the word line WL permits each the access transistors M5 and M6, which causes the bit line BL voltage to either slightly drop m3 is ON and high PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). It ought to be noted that if BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines can have little voltage distinction between them. Ways amplifier can sense that line has the upper voltage and therefore verify whether or not there was 1 or 0 stored. The upper the sensitivity of the sense amplifier, the quicker the browse operation [6].

3. **Writing:** The write cycle begins by applying the value to be written to the bit lines. If we tend to would like to put in writing a zero, we'd apply a zero to the bit lines, i.e. setting BL to one and BL to zero. This is often like applying a reset pulse to an SR-latch that causes the flip flop to alter state. A one is written by inverting the values of the bit lines. WL is then declared and therefore the value that's to keep is secured in. This works as a result of the bit line input-drivers are designed to be much stronger than the relatively weak transistors within the cell itself so that they will simply override the previous state of the cross-coupled inverters. In follow, access NMOS transistors M5 and M6 have to be compelled to be stronger than either bottom NMOS (M1, M3) or high PMOS (M2, M4) transistors. This is often simply obtained as PMOS transistors are much weaker than NMOS once the same sized. Consequently, once one semiconductor combine (e.g. m3 and M4) is only slightly overridden by the write method, the other transistors combine (M1 and M2) gate voltage is additionally modified. This means that the M1 and M2transistors are often easier overridden, and so on. Thus, cross-coupled inverters amplify the writing method [7-8].

II.LITERATURE SURVEY

Liu J et al. [9], proposed 6T shown figure 2 the circuit diagram of a conventional SRAM cell. Before the read operation begins, the bit line (BL) and bit bar line (BLB) is precharged to as high as supply voltage Vdd. When

the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from the supply voltage (Vdd) through the pull-up transistor TP1 of the node storing ''1''. On the other side, the current will flow from the precharged bit bar line to ground, thus discharging a bit bar line. Thus, a differential voltage develops between the BL and BL. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

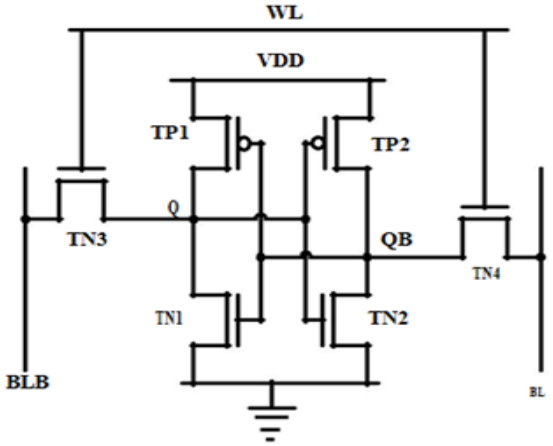

Figure 2: Design 6T SRAM

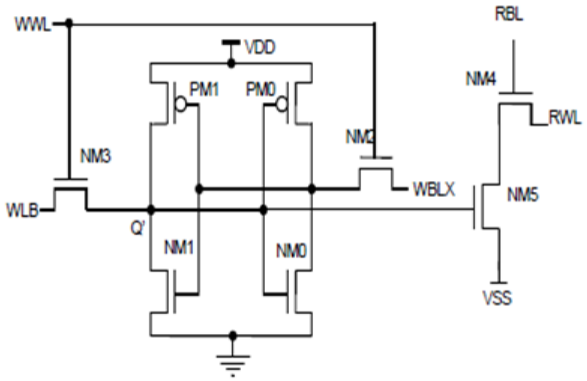

Figure 3: 8T SRAM cell

Shilpi Birla1 et al. [10].Analyzed 8T Static Random Access Memory cell at 65nm process technology is shown in fig.3 This topology was originally proposed for a subthreshold static RAM design and optimized for functionality and performance over a large voltage range. A write operation is performed through WWL, WBL, and WBLX port, whereas single-ended read operation is exercised through RWL and RBL ports.RBL is precharged at the end of each read cycle and keeps precharged during a write cycle. In this bit cell write and read ports are decoupled in contrast to the traditional 6T cell. Read-SNM problem is eliminated and 6T static RAM part can be sized for better writeable without trading off RSNM. This makes the voltage drop across not accessed read buffers zero and hence leakage on the read bit line is highly reduced. Vdd is the virtual supply nodes for the cross-coupled inverters and its voltage can be brought down during write access to weaken PMOS load device and ease write ability problem at low voltage. Since the entire bit cells on a row are written and read at the same time, Vdd is shared across one row of memory cells.

Kursun V. et al. [11]. Introduce 9T SRAM is shown in Fig.4 Write occurs just as in the 6T SRAM cell. Reading occurs separately through N5, N6, and N7 controlled by the read signal (RWL) going high. This design has the problem of the high bit line capacitance with more pass transistors on the bit line.

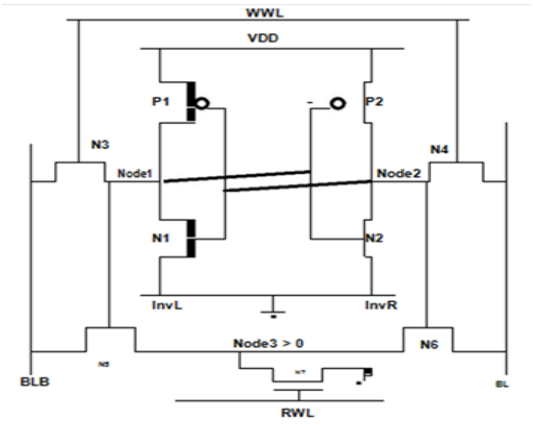

Figure 4: 9T SRAM Cell

III. PROBLEM DECLARATION

In this field, computer memories used storage large data but every device needs power backup .main problem more power dissipation in Static random access memory cell structure. It is a most demandable unit of portable devices like PC, mobile phone and hard disk. The previous dissertation on 6T and 9T the problem of leakage at a cost of degradation in another parameter like read access time, write access time and layout area for 6T, 8T, and 9T. The main purpose of this paper is to reduce power dissipation during the Write operation in the CMOS SRAM cell. Another factor like-cell area, switching delay, power dissipation and how many transistors are used in the implementation of SRAM are also optimizing.

IV.CONCLUSION

Literature review, an extensive survey has been done for various design of Static Random Access Memory. SRAM designs are well preferred for different low power applications. Various techniques to reduce power dissipation have been developed and it can be used for low power and high-speed applications. Design low power dissipation SRAM, low switching delay and less area optimization. It is a basic structure block of the CPU of a computer. SRAM is a structure block of several circuits. Understanding how an SRAM is designed and how it works is essential to building any advanced logic circuits design. Circuits design consists of different kinds of logic invertors, NMOS, and flip-flop. Simply, to operate on bit SRAMs. The micro wind program allows

the designer to design and simulate an integrated circuit at the physical description level.

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