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Enhancing SRAM Cell Circuitry through PDLPDC Optimization

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Abstract: This study focuses on improving static random-access memory (SRAM) cell circuit design by leveraging the Power Dissipation Low Power Dissipation Circuit (PDLPDC). The PDLPDC, a low-power dissipation circuit, has gained widespread use in designing cells for read operations, write operations, and idle modes, contributing to power optimisation in submicron or nano-range Very Large Scale Integration (VLSI) designs. While various SRAM cells, including 6T and 10T configurations, have been developed, they often exhibit higher power consumption. In contrast, our PDLPDC-based approach operates at lower power levels. With the increasing integration of portable devices into everyday life, power optimisation has emerged as a critical challenge in modern VLSI technology. Many contemporary gadgets and systems rely on very Large-scale Integration (VLSI) technology, where static random-access memory (SRAM) blocks occupy substantial chip space and represent a significant source of leakage power in current systems. However, a common practice, scaling the supply voltage of SRAM macros can lead to elevated power dissipation. This research addresses the challenge by efficiently scaling the supply voltage of SRAM macros, resulting in an overall reduction in power dissipation. The study introduces 6T and 10T SRAM circuits that minimise power dissipation during read and write operations while maintaining reasonable performance and stability. The impact of process parameter variations on various design metrics, including read and write power, leakage power, leakage current, and latency, becomes a critical consideration in SRAM cell design with increased integration scale. The proposed circuit, optimised for the minimum power-delay product during read, write, and idle modes, is compared with traditional SRAM cells (6T and 10T) and demonstrates superior performance, reliability, and power efficiency. This research contributes to advancing the understanding of SRAM circuit design, especially in the context of power optimisation and process variations.

Keywords: VLSI, SRAM, LPD, Delay Write, Delay Read, Low Power Dissipation, 6T, 10T, PDLPDC, Power Optimization

I. INTRODUCTION

Memory is a crucial component for storing data or information in electronic devices. Generally, electronic memory devices employ two main types: volatile and non-volatile. The selection between these memory types depends on the specific application, and they play a pivotal role in influencing the speed performance of the devices.

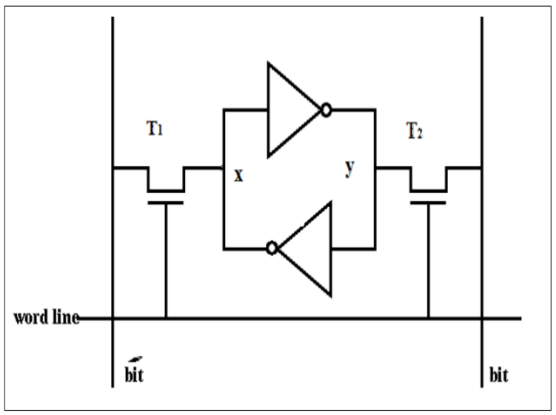

Figure 1. Memory cell

In recent years, Static Random Access Memory (SRAM) has emerged as a significant breakthrough in research, contributing to the enhancement of processing speed while concurrently reducing memory and power demands. This development is essential given the escalating demand for advanced electronic devices like laptops and IC memory cards [1,2]. Cellular feedback mechanisms have been strategically designed to enhance the performance of memory cells [3, 18]. These mechanisms find extensive applications in low-leakage standby on/off memory chip mobile applications. Static memory, integral to semiconductor memory, operates through a bistable latch circuit, enabling the storage of each bit and the display of data memory. It is important to note that static memories fall under the category of volatile

memories, meaning that the stored data is eventually lost when not retained in the memory cell. SRAM, or Static Random Access Memory, represents a type of semiconductor random access memory that utilises latches or flip-flops to store data, with the stored data persisting indefinitely as long as power is consistently applied.

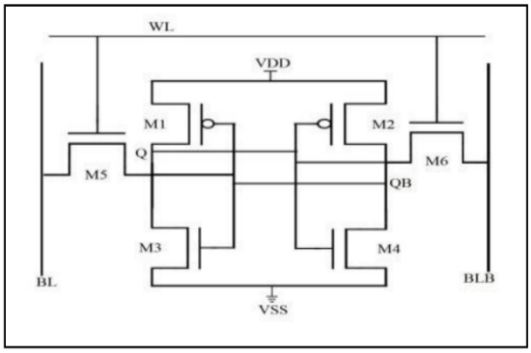

Figure 2. 6T SRAM Cell

In contrast, DRAM, or Dynamic Random-Access Memory, is another type of semiconductor MOS memory that employs a capacitor and a transistor for data storage. Both SRAM and DRAM are categorised as volatile memories. Despite its higher cost and lower packing density than DRAM, SRAM is favoured for its exceptional speed, allowing data to be read from the cell significantly faster than DRAM. Additionally, SRAM does not require periodic refreshing, which distinguishes it from DRAM. Consequently, SRAM is the preferred choice for applications where high speed is essential and the higher cell cost is acceptable, such as in cache memory design. In the current landscape, with the widespread prevalence of portable battery-powered devices, power dissipation and area considerations have become paramount, driving the demand for smaller and more power-efficient devices. As the scale of integration continues to increase to meet the requirements of small-size and high-density chips, the scaling technology introduces operational instability in SRAM cells. Conventional SRAM cells face challenges like leakage current and stability issues in smaller technologies. Various SRAM cell designs have been developed to address these concerns; however, achieving a one-size-fits-all solution is not feasible due to the inherent trade-offs between different parameters of an SRAM cell. Therefore, diverse designs tailored to the specific requirements of various applications have been created, focusing on optimising one or more parameters. This article delves into the discussion of various SRAM cells, each composed of a different number of transistors, highlighting improvement factors over one another and providing an analysis of the advantages and disadvantages inherent in different SRAM cell designs.

Traditional 6T SRAM cells and Standard 6T SRAM Cells utilise two cross-coupled weak inverters to maintain state, along with NMOS transistors functioning as enable signals. These transistors allow the selection of the specific SRAM cell for read/write operations. The cross-coupled inverters serve as memory storage, while the NMOS transistors facilitate read/write operations on designated cells. In this configuration, if the input of the first inverter is logic 1, its output and simultaneously the input of the second inverter are logic 0. The output of the second inverter is then 1, closing the loop. This system operates when the word line transistors are set to 0, effectively isolating the cell from others. An additional advantage of this design is that inverters prevent signal level degradation, eliminating the need for periodic data refresh, a requirement in DRAM technology. The WL line is set to 1, connecting the small line to the inverter to activate a cell for reading or writing. The bit line is the result during a read operation and is the input in a write operation. The latch immediately supports GND and VDD bit voltages. The basic 6T SRAM cell is depicted in Fig. 1. SRAM cells have three working states:

- Operational Maintenance Mode: In standby or maintenance mode (WL=0), access transistors M10 and M6 are blocked, disrupting the bit line series. As long as the SRAM remains in this mode, the data remains unchanged, with a leakage current being the only current flow.
- Read Operation: The SRAM cell must be “enabled” by setting the word line high to execute a read operation. Bitlines are input lines during write operations, with the desired data being altered on the bit line (BL), while BL_inv is driven with the opposite value. For instance, writing a logical ‘0’ involves setting BL to 0 and BL_inv to 1.

The WL (Word Line) signal governs the selection of the SRAM cell. Data transmission occurs through transistors M10 and M6 during a write operation,

wherein transistors M7 and M9 are open, while M6 and M8 are closed. The SRAM cell retains this written value until it undergoes another write operation. In a read operation, WL also needs to be enabled. Before reading data from the SRAM cell, the cell must have a pre-existing value. Activating the cell involves opening transistors M10 and M6 and connecting bl (bit line) and bl_inv (inverted bit line) in series. Preloaded rows are utilised to discern the stored values in memory. Consider the scenario where the SRAM cell has a stored value of 1. M8 and M11 are open in this case, while M9 and M7 remain closed. To read this data, bl and bl_inv are preloaded to high values, and WL is enabled. With M8 open, activating WL does not affect bl. However, in the case of bl_inv, the circuit has a discharge, causing current circulation. Both bl and bl_inv are connected to a sense amplifier acting as a comparator, facilitating the verification of the operation.

II.LITERATURE SURVEY

In this section, we present a comprehensive survey of literature exploring various design strategies for Static Random Access Memory (SRAM) cells, focusing on addressing issues related to leakage current, power consumption, and performance. The following studies contribute significant insights into the advancements in SRAM cell design. Safaryan et al. [8]: The impact of CMOS scaling on sub-threshold leakage, gate leakage, and device variations affecting leakage current is investigated. The study proposes an 8T SRAM cell utilising diode-connected NMOS/PMOS transistors to mitigate leakage current. The proposed circuit demonstrates a threefold improvement in leakage power over the conventional 6T SRAM bit-cell to employ different techniques for leakage reduction. Furthermore, the read and write access times show an enhancement of approximately 18%, with a 10% reduction in power. The experiments use Synopsys Armenia Educational Department's SAED 14 nm technology for FinFET SRAM. Carlson et al. [9]: Figure 3 illustrates a 5T SRAM cell that reduces area by eliminating one access transistor from the conventional 6T SRAM cell. While offering significant reductions in area and power compared to the 6T cell, this 5T cell presents challenges in writing '1', relying on a specific cell sizing strategy for accurate write operations. R. E. Aly et al. [10]: The 7T SRAM cell (Figure 4) introduces an additional NMOS transistor (N5) compared to the conventional 6T SRAM cell. The write operation involves disconnecting the feedback connection between two inverter pairs, with N5 serving this purpose. The 7T cell exhibits improved cell operation and lower write power dissipation. However, the additional transistor increases the cell area by 12.25% compared to the 6T cell. V. K. Tomar et al. [11]: Using the Cadence Virtuoso tool, this study implements various SRAM cell topologies on the 90nm technology node. Results show that the 7T SRAM cell minimises read power, while the 8T SRAM cell achieves a 44.15% reduction in write power compared to the conventional 6T SRAM cell. The write delay in the 9T SRAM cell is the lowest among all considered cells, emphasising the trade-offs in different topologies. L. Chang et al. [12]:

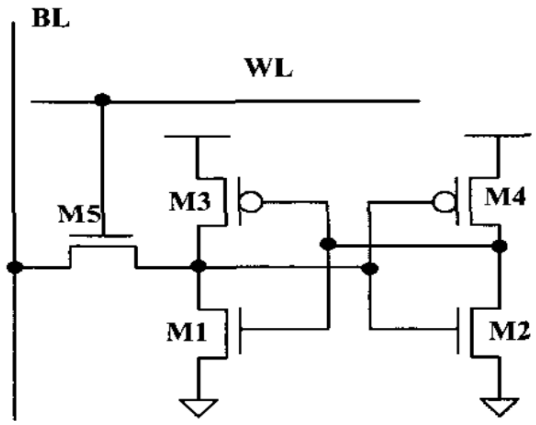

Figure 3. 5T SRAM Cell Schematic

Figure 5 depicts the circuit diagram of an 8T SRAM cell, featuring separate read and write circuits for improved stability and dual-port operation. Despite offering better stability, higher Static Noise Margin (SNM), and lower power consumption, the 8T cell consumes 30% more area on the chip than the conventional 6T cell. Z. Liu et al. [13]: The schematic of a nine-transistor SRAM cell (Figure 6), designed to enhance stability and reduce power consumption, is presented. The cell exhibits 7.7% less leakage power and improved read stability than the typical 6T SRAM cell. However, the cell's larger area consumption and increased read access time are notable disadvantages. N. Arora et al. [14]: In response to the growing demand for memory in the modern era, this study introduces a proposed 10T SRAM cell based on a gated-ground nMOS transistor technique. This technique reduces SRAMs' total leakage power consumption while maintaining

performance. Simulation results across different process nodes (90nm, 45nm, and 32nm) demonstrate the efficacy of the proposed technique in reducing overall power consumption.

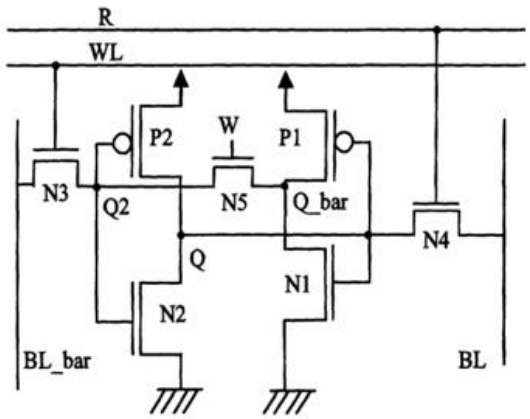

Figure 4. Schematic of 7T SRAM Cell [5]

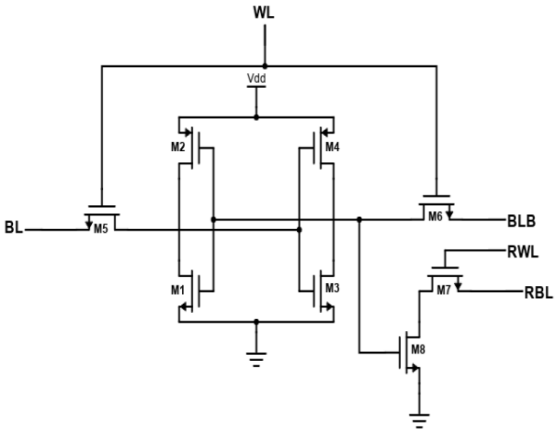

Figure 5. schematic of 8T SRAM cell

III. SOFTWARE MICROWIND TOOLS

Microwind integrates EDA programs that include IC plans from idea to building, allowing chip planners to plan their creative ideas. The Microwind integrates virtually isolated front-end and back-end chip plans into a coordinated flow, accelerating the planning cycle and reducing plan complications. It firmly integrates incoherent and advanced message execution, circuit replication, semiconductor-level mining and confirmation - providing imaginary school conduct to help people and fostering the skills required for configuration positions in virtually all areas of the integrated circuit industry. Microwind Instruments truly coordinates electronic blueprint robotisation programs that integrate IC blueprints from idea to finish, enabling chip mode to plan past creative ideas. Microwind coordinates virtually isolated front-end and back-end chip plans in an integrated flow, accelerating the planning cycle and reducing plan complications.

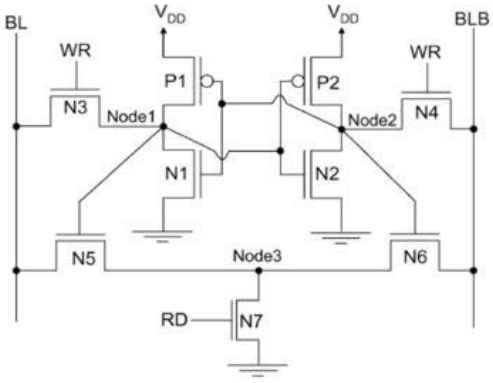

Figure 6. Schematic of 9T SRAM Cell

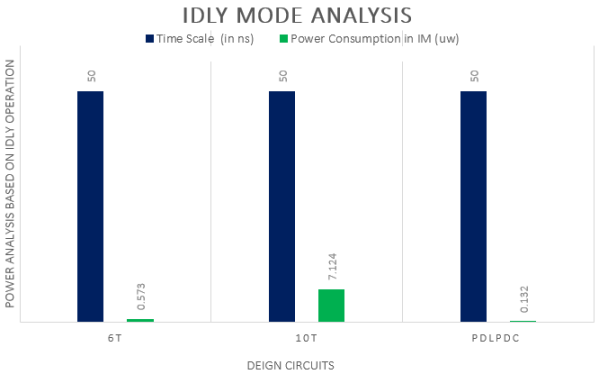

Figure 7. Power consumption analysis between the PDLPDC and 6T,10T in case IM

It firmly coordinates the execution of conflicting message execution and computer execution, circuit reproduction, semiconductor-level mining and verification to provide school conduct invented to help people and promote skills required for the configuration job for all intents and purposes of every space in the integrated circuit industry. The device includes complete switchboards, different perspectives and a simple online test system.

IV. RESULT ANALYSIS

(a) Analysis of Power Consumption in Idle Mode

Figure 7 presents the result graph demonstrating the power consumption analysis during idle operation. The PDLPDC-designed SRAM exhibits a notable reduction in power consumption during idle mode, contrasting with the higher power utilisation observed in the 6T and 10T configurations. In summary, the PDLPDC design is an effective solution, delivering

lower power consumption and enhanced performance in idle mode. The reliability of the PDLPDC-designed SRAM cell circuit is evident in these findings.

(b) Analysis of Power Consumption during Write Operations

The power consumption during write operations is examined in Figure 8, showcasing the effectiveness of the PDLPDC-designed SRAM. This design reduces power consumption during the write mode, outperforming the 6T and 10T configurations and demonstrating higher power usage. Overall, the PDLPDC design stands out for its ability to achieve lower power consumption and superior performance during write operations. These results further affirm the reliability of the PDLPDC-designed SRAM cell circuit.

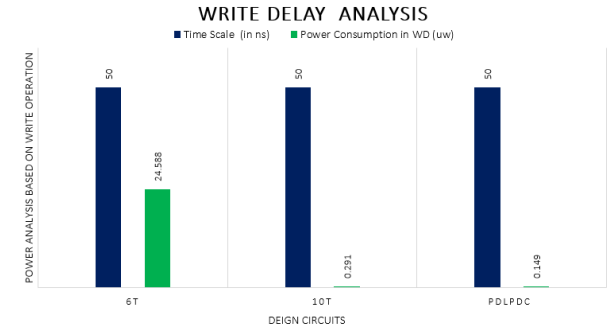

Figure 8 Power consumption analysis between the PDLPDC and 6T,10T in case WM

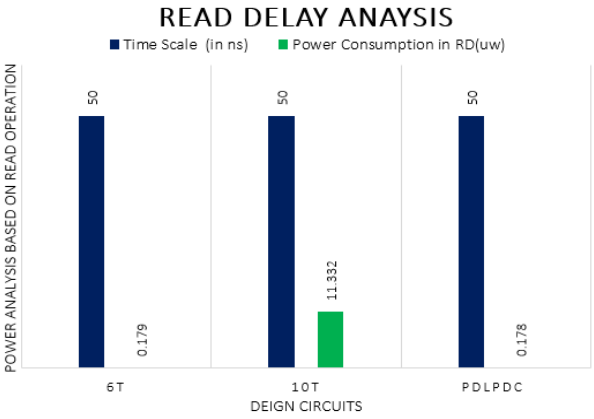

Figure 9 Power consumption analysis between the PDLPDC and 6T,10T in case RM

(c) Analysis of Power Consumption during Read Operations

Figure 9 illustrates the power consumption analysis during read operations for the PDLPDC-designed SRAM, 6T, and 10T configurations. The PDLPDC design substantially reduces power consumption during read mode, surpassing the power usage observed in the 6T and 10T designs. In conclusion, the PDLPDC design consistently demonstrates lower power consumption and superior performance during read operations, emphasising its reliability as an efficient SRAM cell circuit design.

V. CONCLUSION

The enhanced design of the static random-access memory (SRAM) cell circuit, leveraging the PDLPDC concept, marks a significant advancement in addressing power dissipation challenges. The proposed PDLPDC design introduces a low-power dissipation circuit with reliable topology, capable of executing read and write operations, and idle mode with significantly reduced power consumption across a specified frequency range. In contrast, traditional 6T and 10T SRAM configurations exhibit higher power dissipation. SRAM cells are pivotal components in the VLSI domain, but their conventional counterparts suffer from high power consumption. Our study delves into various SRAM cell designs, revealing a trade-off among different parameters during the design process. The existing 6T and 10T SRAM cells are characterised by intricate data storage processes and high power dissipation, which present challenges in achieving power efficiency and speed. The proposed PDLPDC technique overcomes these limitations, enhancing speed while minimising delays. Unlike conventional designs, our approach optimises architecture and peripheral circuits, surpassing traditional device design parameters. The results demonstrate notable improvements in power efficiency during read, write, and idle modes. Energy efficiency is paramount in SRAM cell design, and our PDLPDC-based SRAM cell emerges as a noteworthy contribution. The advancements include a minimised power-delay product during read, write, and idle modes, ensuring high performance, low power dissipation, and circuit reliability. This optimised design underscores the importance of innovative approaches in addressing the evolving challenges associated with SRAM cell technologies.

REFERENCES

[1]. Mahmoodi M. H. M. S., Roy K., “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS

circuits", IEEE proceedings, 91(2), pp. 305–327, 2003.

[2]. Kiran, P. N. V., &Saxena, N. Design and analysis of different types SRAM cell topologies. 2015 2nd International Conference on Electronics and Communication Systems, 2015.

[3]. Choudhari, S. H., &Jayakrishnan, P. Structural Analysis of Low Power and Leakage Power Reduction of Different Types of SRAM Cell Topologies. 2019 Innovations in Power and Advanced Computing Technologies (i-PACT), 2019.

[4]. Preeti S. B., Banakarb R. M. "Implementation of 16X16 SRAM Memory Array using 180nm Technology", International Journal of Current Engineering and Technology, Special Issue 1, 2013.

[5]. Subramanyam J. B. V., Syed Basha S. "Design of low leakage power SRAM using the multi-threshold technique", 2016 10th International Conference on Intelligent Systems and Control (ISCO), 2016.

[6]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Y. Xie, Lowleakage robust SRAM cell design for sub-100 nm technologies, in Proc. ASP-DAC, pp. 539–544, 2005.

[7]. J. Samandari-Rad, M. Guthaus, R. Hughey, Confronting the variability issues affecting the performance of next-generation SRAM design to optimise and predict the speed and yield, IEEE Access 2, 577–601, May 2014.

[8]. Tu, Ming-Hsien, Jihi-Yu Lin, Ming-Chien Tsai, Shyh-Jye Jou, and Ching-Te Chuang. "Single-ended subthreshold SRAM with asymmetrical write/read-assist." IEEE Transactions on Circuits and Systems I: Regular Papers 57, no. 12: 3039-3047, 2010.

[9]. Safaryan, Karo, Mher Bazikyan, Fadey Aslikyan, Stepan Harutyunyan, Garik Hakobyan, and Artur Petrosyan. "Design of Low Leakage SRAM Bitcell." In 2019 IEEE 39th International Conference on Electronics and Nanotechnology (ELNANO), pp. 245-248. IEEE, 2019.

[10]. I. Carlson, S. Anderson, S. Natarajan and A. Alvandpour. A High Density, Low Leakage, 5T SRAM for Embedded Caches, ESSCIRC, 2004.

[11]. R. E. Aly, Md I. Faisal, and M. A. Bayoumi. Novel 7T SRAM cell for low power cache design, in Proc. IEEE SOC Conf., pp. 171–174, 2005.

[12]. V. K. Tomar, D. Mittal, "Performance Evaluation of 6T, 7T, 8T, and 9T SRAM cell Topologies at 90 nm Technology Node," 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Kharagpur, India, 2020, pp. 1-4,2020,

[13]. L. Chang et al. Stable SRAM cell design for the 32nm node and beyond, Proceedings of the IEEE Symposium on VLSI Technology, pp. 128-129, June 2005.

[14]. Z. Liu and V. Kursun. Characterisation of a Novel Nine-Transistor SRAM Cell, IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, Vol. 16, no. 4, pp. 488-492, April 2008.

[15]. N. Arora, S. Singh, N. Gupta and M. Suthar, "Leakage reduction in differential 10T SRAM cell using Gated VDD control technique," 2012 International Conference on Computing, Electronics and Electrical Technologies (ICCEET), Nagercoil, India, pp. 610-614, 2012.

[16]. S. Joshi and U. Alabawi. Comparative Analysis of 6T, 7T, 8T, 9T, and 10T Realistic CNTFET Based SRAM, Journal of Nanotechnology, 2017.

[17]. X. Si et al., "A twin-8T SRAM computation-in-memory unit-macro for multi-bit CNN-based AI edge processors," IEEE J. Solid-State Circuits, vol. 55, no. 1, pp. 189–202, Jan. 2020.

[18]. H. Valavi, P. J. Ramadge, E. Nestler, and N. Verma, "A 64-tile 2.4-mb in-memory-computing CNN accelerator employing charge-domain compute," IEEE J. Solid-State Circuits, vol. 54, no. 6, pp. 1789–1799, Jun. 2019.

[19]. A. Biswas and A. P. Chandrakasan, "CONV-SRAM: An energy-efficient SRAM with in-memory dot-product computation for low-power convolutional neural networks," IEEE J. Solid-State Circuits, vol. 54, no. 1, pp. 217–230, Jan. 2019.

[20]. S. K. Gonugondla, M. Kang, and N. R. Shanbhag, "A variation-tolerant in-memory machine learning classifier via on-chip training," IEEE J. Solid-State Circuits, vol. 53, no. 11, pp. 3163–3173, Nov. 2018.

[21]. E. H. Lee and S. S. Wong, "Analysis and design of a passive switched capacitor matrix multiplier for approximate computing," IEEE J. Solid-State Circuits, vol. 52, no. 1, pp. 261–271, Jan. 2017.