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A Survey on Layout Implementation and Analysis of Different SRAM Cell Topologies

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Abstract: *Because powered widgets are frequently used, the primary goal of electronics is to design low-power devices. Because of its applications in low-energy computing, memory cell operation with low voltage consumption has become a major interest in memory cell design. Because of specification changes in scaled methodologies, the only critical method for the success of low-voltage SRAM design is the stable operation of SRAM. The traditional SRAM cell enables high-density and fast differential sensing but suffers from semi-selective and read-risk issues. The simulation results show that the proposed design provides the fastest read operation and overall power delay product optimization. Compared to the current topologies of 6T, 8T, and 10T, while a traditional SRAM cell solves the reading disruption problem, previous strategies for solving these problems have been ineffective due to low efficiency, data-dependent leakage, and high energy per connection. Our primary goal is to reduce power consumption, improve read performance, and reduce the area and power of the proposed design cell work. The proposed leakage reduction design circuit has been implemented on the micro-wind tool. Delay and power consumption are important factors in memory cell performance. The primary goal of this project is to create a low-power SRAM cell.*

Keywords:- Very Large-Scale Integrated Circuits, Device Circuit, SRAM, Delay Write, Delay Read, power delay product optimization, Low Power Design, Energy Efficient Device.

I. INTRODUCTION

Static random-access memory is semiconductor memory that stores each bit using bistable latching circuitry. The term static RAM distinguishes it from dynamic RAM based on refreshing regularly. SRAM can remember data, but it is still volatile because data is lost when the memory is turned off. Short channel effects, sub-threshold leakage, gate-dielectric leakage, and device-to-device variations are the primary barriers to scaling bulk CMOS to 32nm gate lengths. Because of the abrupt increase in threshold voltage, i.e., Vt oscillation caused by overall and General process variations occur in ultra-short channel devices, 6T SRAM cells, and their modifications, and they cannot be operated at advance supply voltage scaling without functional and parametric failure, resulting in yield loss. The standard 6T SRAM cell design encounters numerous write delay issues. The Low power 6T SRAM cell design reduced write power and access delay but did not improve stability [1]. Memory cells are the basic building blocks of computer memory. The memory cell is an electronic circuit that stores one bit of binary information. It must be set to store logic 1 (high voltage level) and reset to store logic 0 (low voltage level) (low voltage level). Its value is retained/stored until changed.

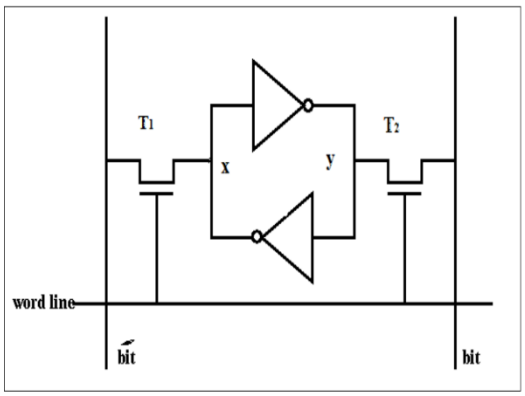

Figure 1 Memory cell

The primary goal of this work is to create a modified SRAM cell with low power consumption. This allows for faster execution and simulation of transistor applications in both analogue and digital domains. FinFET (Fin Field Effect Transistor) is a better option for future nanoelectronics due to its compact susceptibility, high performance, low manufacturing costs, and low power consumption. FinFETs can be used to replace bulk CMOS transistors. Because of its low leakage current and standby power, this technology is an excellent choice for designing memory subsystems. The researchers used the VLSI integration procedure (Very Large-Scale Integration). The procedure by which millions of people VLSI refers to the integration of transistors into a single chip, resulting in an IC (Integrated Circuit). Advances in the field of VLSI have resulted in the rise of innovative technologies that improve circuit speed while minimizing design constraints [2].

1.1 SRAM CELLS AND THEIR OPERATION

SRAM Cell 6T The memory cell is the foundation of any static memory system. Figure 2 depicts a conventional CMOS 6-transistor static memory cell. The circuit

consists of two cross-coupled inverters and two access transistors, M5 and M6 [3].

A. Standby Mode: Because the word line is not asserted in standby mode (word line=0), the pass transistors M5 and M6, which connect the 6t cell to the bit lines, are turned off. It means that the cell is inaccessible. As long as N1 and N2 are connected to the power supply, the two cross-coupled inverters will continue to provide feedback, and data will be stored in the latch [4].
B. READ MODE: The word line (WL) and bit lines (BL) are held at VDD during the read operation. The feedback from the cross-coupled inverters is first broken. Next, by sweeping Q (the inverter's input) from 0 to VDD and measuring QB (the inverter's output), the voltage of the inverter formed by half of the SRAM cell is determined [5].
C. WRITE MODE: VDD is applied to the word line during a write operation, and the value to be written into the memory cell is driven onto the bit lines. As a result, Figure 1 shows how to calculate the write static noise margin (SNM). Again, feedback from the cross-coupled inverters is broken, and the inverter voltage is measured. However, in this case, the voltages of the inverter are calibrated. However, the voltages of the two halves of the SRAM are no longer the same in this case (because one of the bit lines is driven to 0V and the other to VDD) [6].

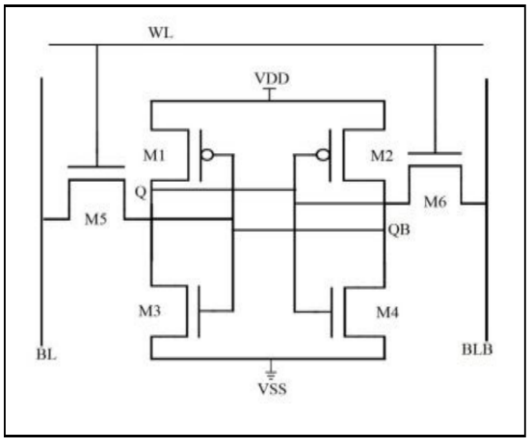

Figure 2 the schematic diagram 6T SRAM Cell

II.LITERATURE SURVEY

K. Takeda et al. [7] described conventional 6T SRAM in which the read operation is performed by pulling the word line high and accessing the latch by access transistors. This may lead to disturbance and corruption of the data stored in the cell due to static noise. Further, in conventional 6T cells, the read operation is quite slow, as activating the access transistors takes undesirable time to access the latch. Slow read operation in SRAM means the time required to respond to a particular operation (read or write) would be large. As a result, the leakage power in the idle circuit would increase over this long period. This reduces the performance of the cell and makes the cell objectionable for use in practical applications. Mishra S et al. [8] design of seven transistors SRAM-cell consists of two CMOS-inverters. These are internally latched with the extra NMOS transistor associated with the read-line, and two NMOS access transistors joined with the bit line bar and bit line individually. Figure 2 of 7T SRAM shows that the M5 access transistor is attached to the word line (WL), which performs the write operation, and the M6 transistor is joined to the read-line (R). The bit line operates as I/O nodes throughout the read-and-write tasks, conveying the information to the sense amplifier.

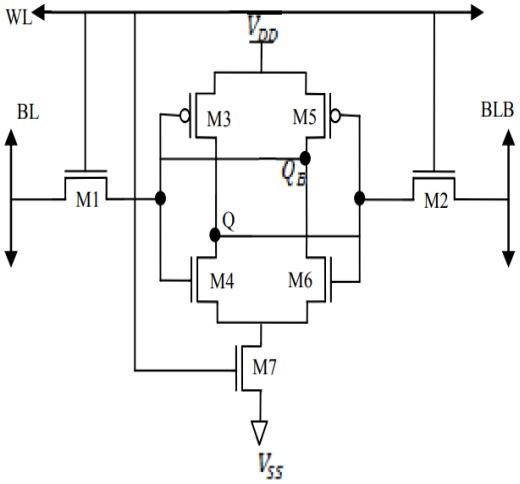

Figure 3 the schematic diagram of 7T SRAM cell

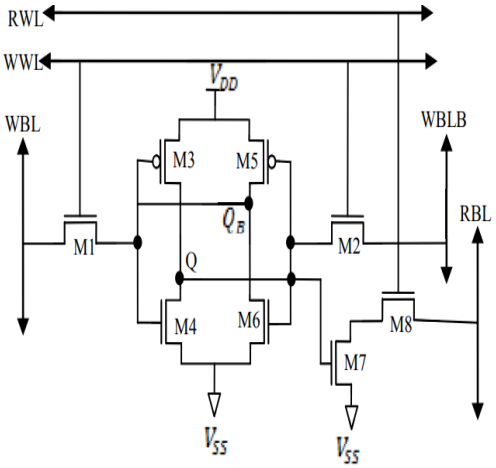

Figure 4 the schematic diagram of 8T SRAM cell

D. Mittal et al. [9] explain 8T SRAM cell addresses several constraints of the 6T circuit, including a separate read port, as shown in Fig.4. The write operation is identical to the 6T circuit, where the write word line (WWL) is charged to turn on the access transistors. Data is applied in the bit lines. Data is stored in the nodes Q and Qb. WWL is set to zero voltage during the read operation, and the read bit-line (RBL) is pre-

charged. When the read word line (RWL) is charged, RBL will discharge through M7 and M8 if '0' is stored in Q ('1' in Qb). When logic '1' is stored. in Q ('0' in Qb), the RBL will not discharge and remain at high logic. Although the write signal can be applied in this circuit during the read function, the RBL must be recharged before the next read operation.

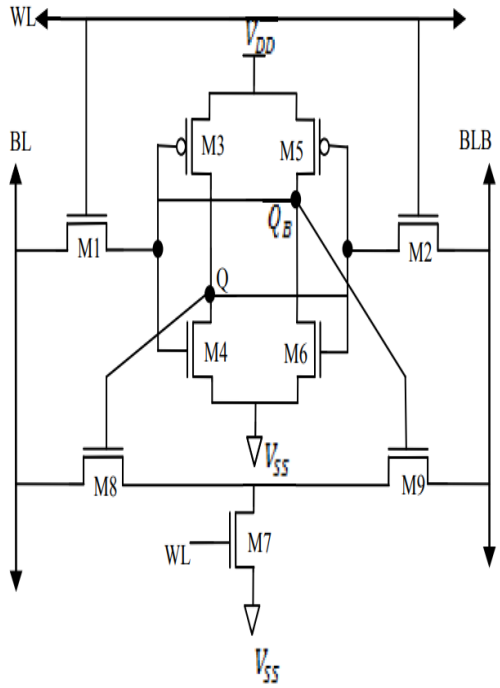

Figure 5 the schematic diagram of 9T SRAM Cell

C. Yu et al. [10] The 9T SRAM cell's architecture consist of the 6T write cell with three additional transistors for the read circuit, as shown in figure 4. The write operation is identical to that of the 6T circuit. The bit lines need to be pre-charged for the read operation, just like in the 6T SRAM cell. However, this time, the bit-lines discharge through M7 or M8 (depending on the stored data of Q and Qb) and M9. The read-line (RL) signal enables the read circuit, and if '1' is stored in Q, the BL is discharged through M7 and M9, while BLB remains at a high state. Since the storage nodes are isolated from the read path, the 9T SRAM cell provides an improved read static noise margin (RSNM) from the 6T SRAM cell. Singh S et al. [11] propose the fully differential low power 10T SRAM bit cell, shown in Figure 5. The design strategy of the cell is the series connection of a tail transistor. The gate electrode of this device is controlled by the output of an XOR gate, inputs of which are tapped from the write word line (WWL) and read word line (RWL) control signals coming from the WWL and the RWL drivers. All the cells in a row share the XOR gate and the tail transistor. The tail transistor has to be appropriately upsized for sinking currents from all the cells in the row. Without this read buffer, a cell with such small drivers and series connected tail transistors would exhibit an unacceptably low read static noise margin (RSNM), resulting in read instability.

III. EXPECT OUTCOMES

The main problem in the Very Large-Scale Integrated Circuits in SRAM like 6T, 8T, and 10T is high power consumption, but our main goal of the proposed layout circuit SRAM cell is to reduce power consumption. Proposed layout circuit SRAM cell, also known as energy efficient SRAM cell, to achieve improved performance, low power consumption, less delay, reliable and best answer.

IV. CONCLUSION

This paper compared the performance parameters of five SRAM cell topologies, which include the conventional 6T, 8T and 10T SRAM cell implementations. In particular, the leakage currents, leakage power and read the behaviour of each SRAM cell are being analyzed. The conventional 6T, 8T and 10T SRAM cells are the most efficient areas with the least transistor count. However, the leakage power becomes large, and the read stability decreases due to the undesirable time the basic latch consumes to read the cell during the read operation. Moreover, the cell data is prone to corruption due to external noise. These models show a significant reduction in the leakage current and power dissipation compared with conventional MOSFET-based SRAM cells. The leakage currents, leakage power, and read behaviours of each SRAM cell are specifically examined. The conventional 6T, 8T, and 10T SRAMs have the fewest transistors and take up the least space. The proposed design circuit development focuses on the electronic devices' limited use of supply voltage. As a result, recent integrated circuits have design requirements that limit power consumption with new architectures. The proposed leakage reduction design circuit has been implemented on the micro-wind tool. Delay and power consumption are important factors in memory cell performance. The primary goal of this project is to create a low-power consumption SRAM cell.

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