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Design and Analysis of Comparator using Adiabatic ECRL and PFAL Techniques

Ravneet Kaur, Er. Ashwani Kumar Singla
PG Scholar, Yadvindra College Of Engg., Talwandi Sabo, Punjab
Assistant Professor, Yadwindra College of Engg, Talwandi Sabo, Punjab

Abstract

The most important mean for design VLSI circuits have been amount of power dissipates throughout these circuits. Therefore adiabatic techniques like ECRL & PFAL used for low power circuit design come into being. Within this paper I am going to discuss two most important adiabatic logic designs ECRL and PFAL. 2-Bit comparator is implemented by these design techniques and results are compared such as transistor count, and average power consumption and delay. The designing of schematic and simulation of circuit are done on tanner tool v13. Since the results it is found to the output level designed for PFAL are improved as compare to ECRL base circuit.

Keywords –Tanner, ECRL, PFAL, Adiabatic, Comparator

Introduction

With the express development into semiconductor technology, the operation speed of CMOS chips have been raising, so that power consumption has become a critical concern within VLSI circuit. Since lots of the present day electronic devices are moveable, they want extra battery backup which can be achieve just with the low power consumption circuits that are internally intended during them. As a result energy efficiency has become most important concern into the convenient equipments to get enhanced performance with less power dissipation. The identical as the power dissipation into an appliance increase then additional circuitry is needed to cool the device and to protect the device from thermal breakdown which also results in increase of total part
of the device. In order to overcome these troubles the power dissipation of the circuit is to be reduced by adopt dissimilar low power technique. The lesser amount of the power dissipation, the more proficient the circuit will be. The dynamic power involve, CMOS circuits is quickly becoming an input concern in the design of personal information system all along by huge computer. A novel CMOS logic family called Adiabatic Logic; base on the adiabatic switching principle is obtainable. [7] The adiabatic circuit that utilizes AC power supplies to reprocess the charge of node capacitances is a mostly attractive approach to diminish power dissipation.

Adiabatic logic

Adiabatic logic is a realization of reversible logic into CMOS wherever the current flow throughout the circuit is controlled such with the purpose of the power dissipation due to switching and capacitor dissipation be minimize .The word adiabatic refers to thermodynamic processes which do not dissipate any heat to the environment. The application of thermodynamic principle of adiabaticity into the circuit design is based upon following two principles: (1) Never turn on transistor as there is a voltage potential between the sources and drain terminal, and (2) Never turn off a transistor when current is flowing through it. Adiabatic logic offers a way to reuse the energy stored in load capacitor rather than discharging the load capacitor to the ground and wasting this energy. [2] Adiabatic logic family can be generally classified as:

Fully Adiabatic – In fully adiabatic circuits, all the charge on the load capacitance is improved with feedback to the power supply. This makes the fully adiabatic circuits slower and more complex as compare to partially adiabatic circuit. Pass transistors adiabatic logic (PAL) and split-rail charge recovery logic (SCRL) techniques are popular fully adiabatic logic techniques.

Partially Adiabatic -- In partial adiabatic or quasi adiabatic circuits, a few charge is allowed to be transfer to the ground i.e. some heat is dissipated hence a part of energy only being able to recover, but these circuits are easy to implement as compared to fully adiabatic logic Efficient charge recovery logic (ECRL) plus positive feedback adiabatic logic (PFAL) are common examples of quasi adiabatic techniques .[2]

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ECRL – Efficient charge recovery logic

Efficient charge recovery logic significant logic families and be helpful for low energy system. Its structure is based upon standard CMOS family known as Differential Cascade Voltage Switch Logic (DCVSL). ECRL planned by Moon and Jeong, this arrangement use pair of pull-down NMOS devices to evaluate logic function along with two cross-coupled PMOS transistors to hold the status. Whole recovery of power clock is not possible throughout PMOS devices, thus it is still quasi-adiabatic logic technique.

ECRL is base around a couple of cross- coupled PMOS transistors. Their source terminal are coupled in the direction of the power - clock, and the gate of each one is connected toward the drain of the others. These nodes are from the complementary output signals. The function is evaluated by a series of pull- down NMOS devices. [1]

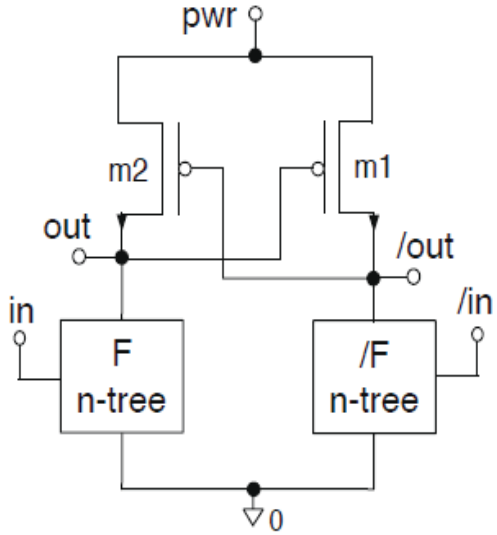

Fig. 1 Basic ECRL Structure

The designing of circuit is done by following steps:

- Make the truth table for the desired circuit, combine the case for 1's and 0's separately and make Boolean equation for both.
- Draw the cross- coupled PMOS structure.
- Replace N- tree structure below out terminal with circuit for Boolean equation of 0 and N-tree below /out with circuit for Boolean equation of 1.

Working of the circuit is as following:

- For the cases of 0's the F n-tree will work and we will get 0 potential at out. This 0 will make transistor m1 ON and the /out terminal will follow the clock.
- For the case of 1's the /F n-tree will work and we will get 0 potential at /out terminal. This 0 will make transistor m2 ON and the out terminal will follow the clock.

PFAL – Positive feedback adiabatic logic

This circuit has smaller amount power consumption. It is partial adiabatic system with dual railing. PFAL circuit consist of an adiabatic amplifier, a latch made by two PMOS and two NMOS, which avoid the logic level degradation on the out and /out. The two n- trees realize the logic functions. The logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of adiabatic amplifier and form a transistor gate. PFAL uses four phase clock. [1]

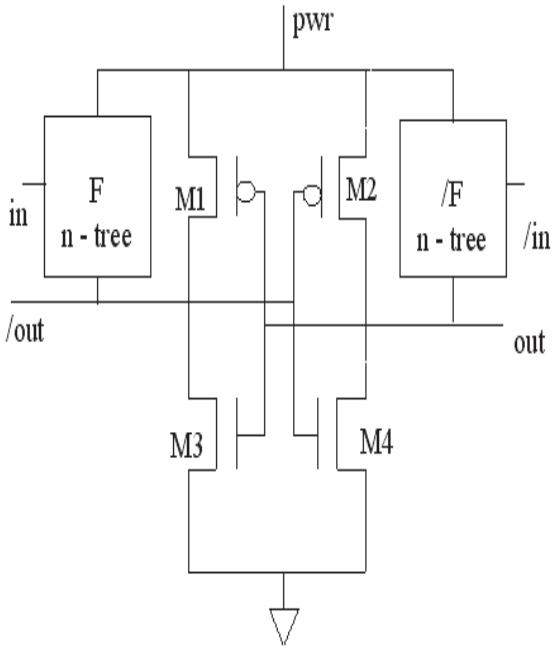

Fig. 2 Basic PFAL structure

The designing of circuit is done by following steps:

- Make the truth table for the desired circuit, combine the case for 1's and 0's separately and make Boolean equation for both.
- Draw the cross- coupled PMOS structure.
- Replace N- tree structure below out terminal with circuit for Boolean equation of 0 and N-

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- For the case of 1's the /F n-tree will work and we will get 0 potential at /out terminal. This 0 will make transistor m2 ON and the out terminal will follow the clock.

Expression for comparator circuit

Two -bit Comparator

2-Bit Magnitude Comparator Compares two numbers each having two bits (A1, A0 & B1, B0)

For A>B: = A1B1‟+A0B0‟A1‟B1‟+A0B0‟A1B1
= A1B1‟+A0B0‟(A1‟B1‟+A1B1) = A1B1‟+A0B0‟ X1

For A=B: = A1‟A0‟B1‟B0‟+ A1‟A0B1‟B0+A1A0‟B1B0‟+A1A0B1B0
= (A1‟B1‟+A1B1) (A0‟B0‟+A0B0)
= X1X0

For A<B: = A1‟B1+A0‟B0A1‟B1‟+A0‟B0A1B1
= A1‟B1+A0‟B0 (A1‟B1‟+A1B1)
= A1‟B1+A0‟B0 X1

Truth table of comparator

INPUT				OUTPUT		
A1	**A0**	**B1**	**B0**	**A>B**	**A=B**	**A<B**
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

According to logic function obtained from truth table, the logic diagram is drawn as follows

Inputs A= A0A1

B=B0B1

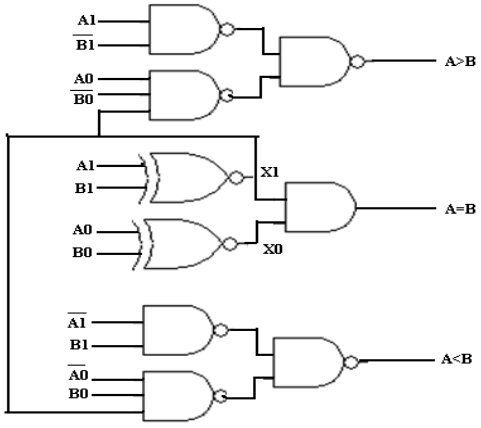

Fig. 3 logic diagram of 2- bit magnitude comparator

Circuits and simulations:

Results of Comparator circuit using ECRL: simulation wave form of two bit comparator using ECRL

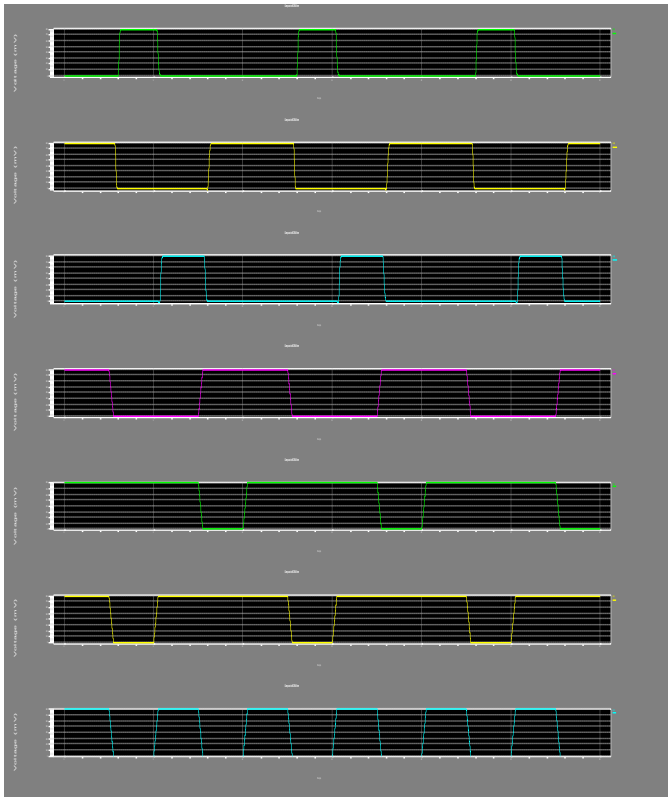

Fig.4 output waveform of Comparator Using ECRL

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Simulation wave form of two bit comparator using PFAL

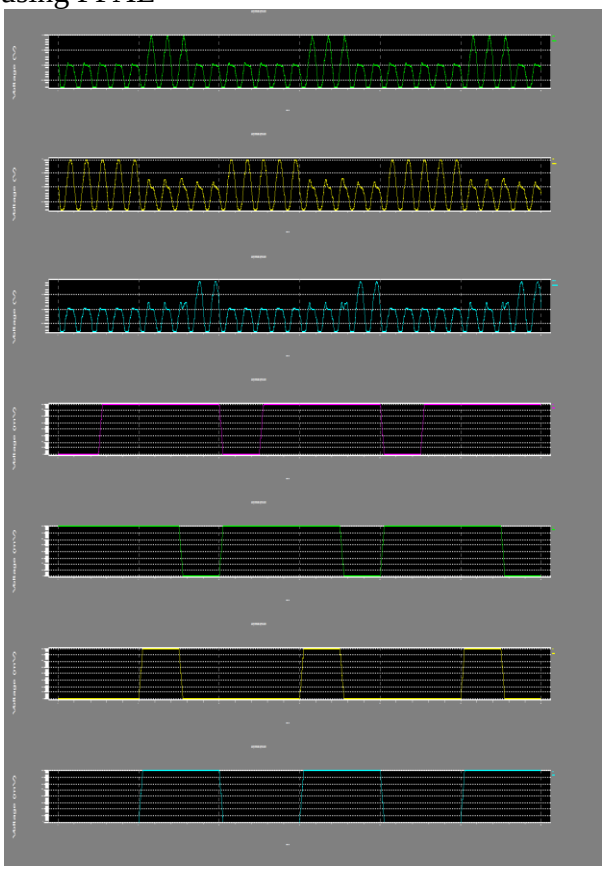

Fig 5 Output waveform of 2-bit comparator using PFAL

Table 1 Transistor count & delay of 2-bit comparator

	ECRL	PFAL
Transistor count	110	92
delay	3.5053e-010	4.6139e-010

Table 2 Power consumption chart of 2-bit comparator

Frequencies	ECRL Power consumed (µw)	PFAL Power consumed (µw)
500 MHZ	30.61850	9.854761
200 MHZ	26.85715	3.291794
100MHZ	23.73231	1.634717

Conclusion

We implemented the two bit comparator circuit using ECRL and PFAL techniques. Through the implementation we compared two techniques with respect to transistor count, maximum operating frequency, power dissipation and output level quality. Transistor count of 2- bit comparator 110 and 92 respectively ECRL and PFAL. It is fount that for 90nm technology ECRL based two bit 2-Bit comparator circuit dissipates max power of 30.61850µw at 500 MHz and least power 23.71225µw at 100MHz. The PFAL based circuit dissipates max power at 9.854761µw at 500 MHz and least power 1.634717µw at 100Mhz.The output level of PFAL are better as compared to ECRL based 2- Bit comparator using 90nm technology.

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Authors

First Author – **Ravneet Kaur**, PG Scholar, VLSI Design, Yadvindra College of Engineering, Talwndi Sabo, Punjab.

Second Author – **Ashwani kumar Singla**, Assistant Professor, Department Of ECE, Yadvindra College Of Engineering, Talwandi Sabo, Punjab.