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MODIFIED QUATERNARY DIVISION OPERATION BASED ON TERAHERTZ OPTICAL ASYMMETRIC DEMULTIPLEXER

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Abstract

Modified Quaternary division based on all Terahertz Optical Asymmetric Demultiplexer (TOAD) is proposed. It shows quaternary division operation based on compact detect-zero circuit using T-gate. In this present work all optical scheme of the different quaternary logical states are represented by different polarized state of light. Introducing the compact detect-zero circuit reduces the overall number of the T-gates in the division operation and the number of T-gate incoming data transmission lines to three. The design promises both higher processing speed and accuracy. The design can be evolution for more complex optical circuits of enhanced functionality in which the T-gate is the basic building block. Numerical simulation result of all optical quaternary division circuits by MATLAB confirming described method is given in this paper

Introduction

The field of computation and information processing is growing day by day. In last few decades, the philosophy, science and technical prospects enriched the scientific communities a lot. Massive parallelism, speed of operation, increased spatial density attract in many ways to the scientists, researchers and technologists. In order to overcome the electronic bottlenecks and fully exploit the advantages of optics, it is necessary to move towards networks, where the transmitted data will remain exclusively in all optical domains without optical electrical optical (OEO) conversions [1]. Ultra high-speed optical network is developing rapidly as growing capacity demand in telecommunication system is increasing. In these networks, it is desired to carry out switching, routing and processing in optical domain to avoid bottlenecks of optoelectronic conversions. The dream of photonics is to have a completely all-optical technology.

All optical logic operations have many potential applications in optical communication and computing systems. Various architectures, algorithms, logical and logic operations have been proposed in the field of optical/optoelectronic computing and parallel signal processing in last few decades [2]. Photon is the ultimate unit of information with unmatched speed and with data package in a signal of zero mass, the techniques of computing with light may provide a way out of the limitations of computational speed and complexity inherent in electronics computing [3].

Chattopadhyay and Roy proposed a novel all-optical quaternary successor (QSUC) circuit with the help of semiconductor optical amplifier (SOA)-assisted Sagnac switch. All-optical successor circuit can take an important and significant role in designing of all-optical quaternary universal inverter and modulo arithmetic unit (addition and multiplication) [1].

Gayen et al. propose and describe the TOAD-based switch to design an integrated circuit which can perform the addition of two 2-bit numbers in all-optical domain. An all-optical model of carry look ahead adder (CLA) implemented with a semiconductor optical amplifier (SOA)-assisted Sagnac interferometer (TOAD) is presented [4]. Chattopadhyay and Roy proposed an all optical scheme of polarization encoded quaternary (4- valued) MAX logic gate with the help of Terahertz Optical Asymmetric Demultiplexer (TOAD) based fiber interferometric switch is described. For the quaternary information processing in optics, the quaternary number (0, 1, 2, and 3) can be represented by four discrete polarized states of light [5].

Moniem and C. proposed the implementation of binary decoder and encoder and using the optical hardware components. All-optical circuits are implemented and designed with nonlinear material such as terahertz optical asymmetric demultiplexer (TOAD) in optical tree architecture, polarization converters, and optical circulator. Multi-valued logic can be used as an alternative approach to solve many problems in transmission, storage and processing of large amount of information in digital signal processing. A suitable number system and an efficient encoding/decoding scheme for handling the data are very essential to achieve the parallelism in computation. Device-based simulation of the proposed optical

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circuit is used to verify the operation of the optical converter [6].

Among the proposed schemes, the terahertz optical asymmetric demultiplexer (TOAD)/semiconductor optical amplifier (SOA)-assisted Sagnac gate effectively combines fast switching time and a reasonable noise figure, with the ease of integration and overall practicality that enables it to compete favorably with other similar optical time division multiplexing (OTDM) devices. TOAD is characterized by the attractive features of fast switching time, high repetition rate, low power consumption, low latency, noise and jitter tolerance, compactness, thermal stability and high nonlinear properties, which enable their efficient exploitation in a real ultra-high speed optical communications environment. TOAD have the potential of being integrated, which in turn means that they can be repeatable and reliably manufactured and massively produced so that they can be of commercial value and favorably compete with other buffering solutions [7].

TOAD is operationally versatile, i.e. they can be exploited in more complex all-optical signal processing applications without significantly changing their fundamental architecture. In this communication we propose the TOAD-based switch to design an integrated all-optical circuit which can perform different logical operations.

In this paper the quaternary division structure with detection circuit of zero number has been presented. The structure of quaternary division based on (TOAD) used to design T-gate. Minimum number of T-gates is used to set the design. The paper is organized as follows. The principle and operation of TOAD based optical switch is discussed then, the design and operational principle of some basic all-optical quaternary logic circuits (QMIN, Delta Literal) and describes the principle of T-gate and its operation. Detect-zero circuit is discussed alone with its design and operational principle. Quaternary division operation with compact detect zero circuit simulation results and discussion is presented. Finally, conclusion and suggests a roadmap for future works are discussed.

Operational principle of TOAD based all-optical switch

Quaternary logic (R =4) has four logical states {0, 1, 2, 3}. In optics, the quaternary number has been represented by four discrete polarized state of light. In optical implementation we can consider the set of quaternary logic states {0, 1, 2, 3}:

0 = no light,

1 = vertically polarized light (↕),

2 = horizontally polarized light (●) and

3 = partially polarized light (⇳).

Like binary world there are also numbers of basic gates in multi-valued logic world. Depending on the radix and number of variables used, different logic functions can be generated. The numbers of possible functions are [8]:

$$f\ (R,n) = R^{(R)^n} \qquad (1)$$

where R is the radix and n is the number of variables, in quaternary logic (R=4) of two variables (n=2), there are $f\ (4,2) = 4^{4^2}$ = 4294967296 possible functions. Among the proposed schemes, TOAD / SOA-assisted Sagnac gate effectively combines fast switching time and a reasonable noise figure, with the ease of integration and overall practicality that enables it to compete favorably with other similar optical time division multiplexing (OTDM) devices [9].

TOAD are characterized by the attractive features of fast switching time, high repetition rate, low power consumption, low latency, noise and jitter tolerance, compactness, thermal stability and high nonlinear properties, which enable their efficient exploitation in a real ultra-high speed optical communications environment. TOAD have the potential of being integrated, which in turn means that they can be repeatably and reliably manufactured and massively produced so that they can be of commercial value and favorably compete with other buffering solutions.

The TOAD consists of a loop mirror with an additional, intraloop 2 X 2 3dB coupler, and a SOA that is offset from the loop's midpoint by a distance Δx as shown in Fig. 1(a). The TOAD has two inputs input pulse (IP) and control pulse (CP). The operation can be explain when an input pulse (IP) enters the loop through the main coupler and produces two pulses in the loop; a clockwise (CW) propagating pulse and a counterclockwise (CCW) propagating pulse. As they traverse the loop, the CW pulse and the CCW pulse are always located on opposite sides of the loop, equidistant from the midpoint. Each passes through the SOA once, and they return to the main coupler at the same time. A control pulse (CP) injected into the loop via the intraloop 2 X 2 coupler passes once through the SOA, and then passes out of the loop. The CP has sufficient energy to significantly modify the optical properties of the SOA, but the CW and CCW signal pulses do not.

The output power at Transmitted port (T-port) and Reflected port (R-port) can be expressed as :

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$$P_T(t) = \frac{P_{in}}{4}(t).\{G_{cw}(t) + G_{ccw}(t) - 2\sqrt{G_{cw}(t) + G_{ccw}(t)}\cos(\Delta\Phi)\} \quad (2)$$

$$P_R(t) = \frac{P_{in}}{4}(t).\{G_{cw}(t) + G_{ccw}(t) + 2\sqrt{G_{cw}(t) + G_{ccw}(t)}\cos(\Delta\Phi)\} \quad (3)$$

where, $G_{cw}(t), G_{ccw}(t)$ are the power gain and the phase difference between cw and ccw pulse [10], $\Delta\Phi = -\alpha/2\ln(G_{cw}/G_{ccw})$, α is line-width enhancement factor. In the absence of a control signal, IP enters the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and experience the same unsaturated amplifier gain G_0 of SOA, recombine at the input coupler i.e. $G_{ccw} = G_{cw}$, Then, $\Delta\Phi = 0$. So expression for $P_T(t) = 0$ and $P_R(t) = P_{in}(t)G_0$. It shows that data is reflected back towards the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. As a result, cw and ccw will experience differential gain saturation profiles i.e. $G_{ccw} \neq G_{cw}$. Therefore, they recombine at the input coupler, and then $\Delta\Phi \approx -\pi$ the data will exit from the transmitted port i.e. $P_T(t) \neq 0$ and $P_R(t) \approx 0$, the corresponding values can be obtained from eq. (2) and eq. (3).

a)

b)

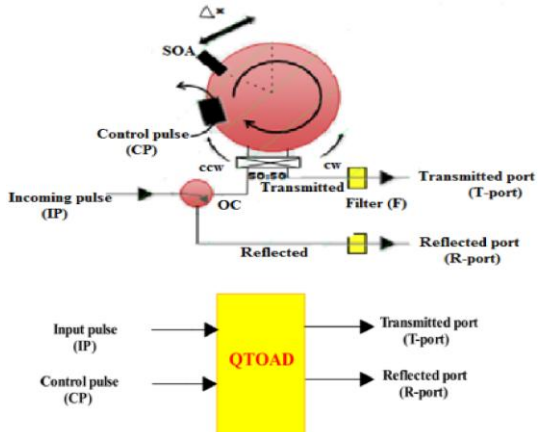

Figure 1. Terahertz optical asymmetric demultiplexer (TOAD) based switch. (a) Schematic diagram; CP: control pulse, SOA: semiconductor optical amplifier, OC: optical circulator, which separates the reflected light from the loop to R-port and (b) block diagram.

The principle operation of TOAD can be described as:

Case1: CP=ON, then SOA changes its index of refraction. As a result, cw and ccw will experience a differential gain saturation profiles. Therefore, cross phase modulation (XPM) takes place when they recombine at the input coupler. Then, relative phase difference between cw and ccw pulses becomes π and the data will exit from the transmitted port (T-port) according to Fig.1 (b).

Case 2: CP=OFF, cw and ccw enter the fiber loop, pass through the SOA at different times counter-propagate around the loop, it experience the nearly same unsaturated amplifier gain of SOA, and then they recombine at the input coupler. Relative phase difference between cw and ccw is zero (0), and no data is found at the T-port. Then data is reflected back toward the source and isolated by optical circulator (OC) [11].Table-1 describe the operation of TOAD.

Table 1. Truth table of TOAD operation

Incoming pulse(IP)	Control pulse(CP)	T-port	R-port
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

APPLICATIONS OF TERAHERTZ OPTICAL ASYMMETRIC DEMULPLEXER

A. Design of two inputs all-optical quaternary MIN (X, Y) circuit

The QMIN operation is shown in eq. (4), the operator $\wedge$ is QMIN operation.

$$x_1 \wedge x_2 \wedge \ldots\ldots\ldots \wedge x_n = QMIN(x_1, x_2, \ldots\ldots\ldots, x_n) \quad (4)$$

A QMIN(x, y) function is shown in table-2, and the optical circuit is shown in Fig. 2. Here light from inputs X and Y fall on two polarization beam splitter (PBS_1 and PBS_2), where it split into two polarized light one is vertically polarized (↕) and the other is horizontally polarized (●). X_1, Y_1 are vertically polarized (↕), and X_2, Y_2 are horizontally polarized (●). Light from X_2 and Y_2 are fed to two switches S_1 and S_2 as incoming signal, and also their control signals have taken from Y_2 and X_2, respectively. The lower outputs of S_1 and S_2 are passed through a polarization converter (pc) which is preferably half wave plate ;converts vertically polarized light

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to horizontal one and vice versa. It is indicated as S_{1L} and S_{2L}, respectively. Then, X_1 and S_{1L} are combined by a beam combiner BC-1, and the combined ray (C_1) is connected to another switch S_3 as incoming signal. Also, Y_1 and S_{2L} are combined by BC-2, and the combined ray (C_2) is connected to S_3 as control signal. The upper output channel of S_3 (S_{3U}) is fed to BC-3. Again X_2 and Y_2 are fed to another switch S_4 as incoming and the control signal ,respectively [12]. All the control signals are amplified by an erbium-doped fiber amplifier (EDFA) [13].When the incoming light signal is incident on the wavelength converter (WC), it converts the wavelength of the incoming signal to wavelength of the control signal. The upper output channel of this switch S_4 (S_{4U}) is connected to BC-3. The combined ray is the final

output [12].

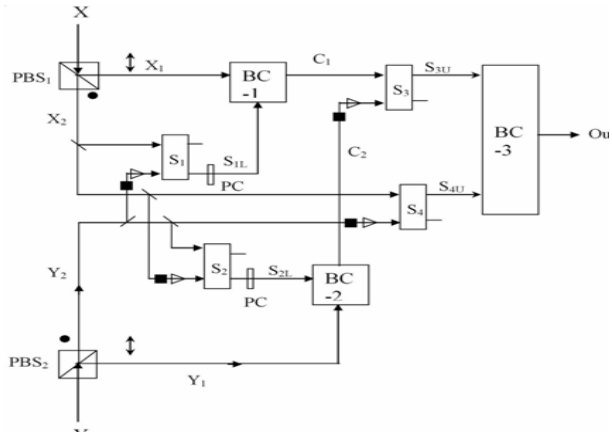

Figure 2. All-optical quaternary QMIN(X, Y) circuit. S: switch, NOLM: Non-linear optical loop mirror, PBS: polarizing beam Splitter, BC: beam Combiner, PC: polarization converter, ► EDFA: erbium doped fiber amplifier, ■ wavelength converter [12].

The operational principle of quaternary minimum is illustrated as:

CASE1: X=0, $X_1=X_2=0$, if Y=0; $Y_1=Y_2=0$ then $S_{1L}=C_1=S_{2L}=C_2=S_{3U}=S_{4U}=O/P=0$. Therefore, for different values of Y<123> the output is 0 (no light).

CASE 2: X=1, $X_1=1$, $X_2=0$, if Y=0; $Y_1=Y_2=0$ then, $C_1=1$, $S_{1L}=C_2=S_{2L}=S_{3U}=S_{4U}=O/P=0$. For different values of Y<123>, the output is 1 (vertical polarized light).

CASE 3: X=2, $X_1=0$, $X_2=2$, if Y=0; $Y_1=Y_2=0$ then, $S_{IL}=C_1=2$, $S_{2L}=C_2=S_{3U}=S_{4U}=O/P=0$. For values of Y<23>, the output is 2 (horizontal polarized light) but if the value of Y is 1 then, the output is 1 (vertical polarized light).

CASE 4: X=3, X1=1, $X_2=2$, if Y=0; $Y_1=Y_2=0$ then, $S_{2L}=C_2=S_{3U}=S_{4U}=0$, $S_{1L}=2$, $C_1=3$ and the output is 0. For the different values of Y <123> output equals to the value of Y.

Table 2. Truth table of quaternary MIN(X, Y)

X \ Y	0(Z)	1(↕)	2(●)	3(◆)
0(Z)	0	0	0	0
1(↕)	1	1	1	1
2(●)	1	1	2	2
3(◆)	1	1	2	3

B. Design of all optical quaternary Delta Literal circuit

Literals are very important function in multi-valued logic based information processing. The truth table of Delta literal circuit is in the table- 4 and the circuit diagram is shown in the Fig. 3. Here, X is the quaternary input, which can take any one of the four quaternary logic states <0123> and the outputs are x^0, x^1, x^2 and x^3, respectively [3].

Table 3. Truth table of quaternary Delta Literals

X \ O/P	X^3	X^2	X^1	X^0
0 (z)	0	0	0	3
1(↕)	0	0	3	0
2(●)	0	3	0	0
3(◆)	3	0	0	0

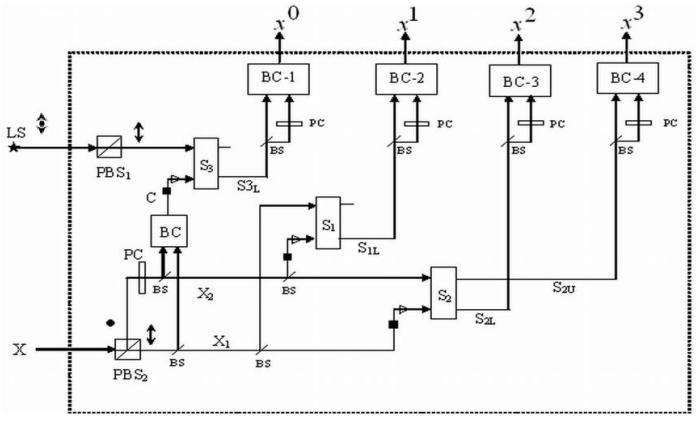

Figure 3. All optical quaternary delta literal circuit [13].

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The operation of quaternary delta literals is briefly described in table 4.

Table 4. Truth table of operational principle of quaternary delta literal

X	X_2	X_1	S_{1L}	S_{2U}	S_{2L}	S_{3L}	X^3	X^2	X^1	X^0
0 (z)	0	0	0	0	0	1	0	0	0	3
1 (↕)	0	1	1	0	0	0	0	0	3	0
2 (●)	1	0	0	0	1	0	0	3	0	0
3 (♦)	1	1	0	1	0	0	3	0	0	0

C. Quaternary T-gate

This T-gate is successfully used for designing any quaternary circuits, so it is called 'universal' element of quaternary logic. Schematic diagram for quaternary T-gate is shown in Fig. 4.

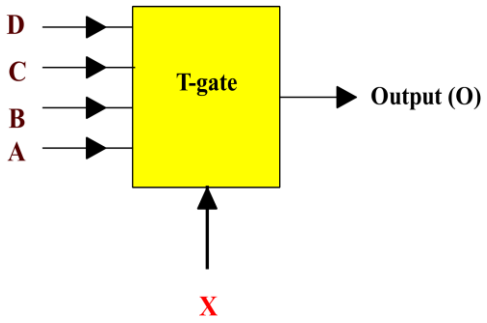

Fig.4. All optical Quaternary T-gate.

The four incoming data transmission lines are 'A', 'B', 'C' and 'D' [which can be any one of the 4-logical state i.e. 0 (no light), 1(↕), 2 (•), 3 (♦)] and 'X' is the selection input. By using proper section we can get any data (A, B, C or D) at the output. If X=0, the output is A, when X=1 then the output is B, for X=2 the output is C and when X=3 then the output is D respectively [3].

$$T(A,B,C,D)=\begin{cases}A & if\ x=0\\ B & if\ x=1\\ C & if\ x=2\\ D & if\ x=3\end{cases} \quad (5)$$

The mathematical expression for all-optical quaternary T-gate using MIN & delta literals can be written as [14]:

$$O=(A\wedge x^{<3000>}+B\wedge x^{<0300>}+C\wedge x^{<0030>}+D\wedge x^{<0003>}) \quad (6)$$

x ∧ y= minimum of (x, y) and δ- literals function is x^{a} = (R − 1) if x=a, else 0.

Compact Detect-Zero Circuit

The number 'zero' is undesirable in division operation, which causes the output to be undefined when it's placed in the denominator. Therefore, a zero detect circuit is necessary for each input before entering the operation.

The block diagram of a proposal quaternary detect zero is shown in Fig. 5 which uses three T-gates.

The operation of compact detect- zero circuit depends on the value of D. If D=0, the quaternary input X can be checked and if D=1, the quaternary input Y is checked.

When X or Y entered to T-gate1 the O_1 is quaternary number has four states which are no light (0), vertical polarization light (1), horizontal polarization light (2), and partial polarization light (3). T-gate2 depends on O_1 and its output called zero output (O_z), if O_1 equal to zero, O_z is zero else, O_z is NaN. T-gate3 depends on O_1 and its output called non zero output (O_{nz}), if O_1 equal to zero, O_{nz} is NaN else, O_z is <123>.

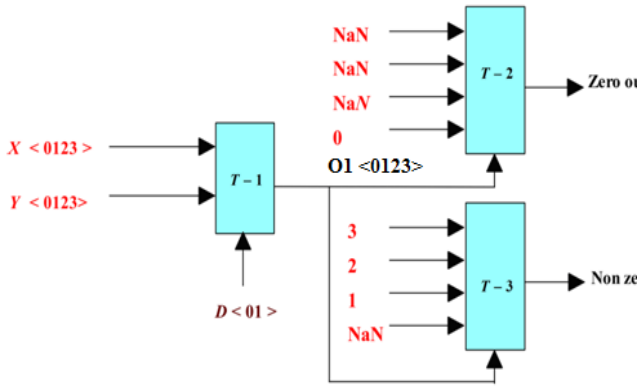

Figure 5. Quaternary detect-zero circuit

The selection outputs (O_1, O_z, O_{nz}) of the three T-gates which are used in the design can be expressed as

$$O_1=(X\wedge D^{<30>}+Y\wedge D^{<03>}) \quad (7)$$

$$O_z=(0\wedge O_1^{<3000>}+NaN\wedge O_1^{<0300>}+NaN\wedge O_1^{<0030>}+NaN\wedge O_1^{<0003>}) \quad (8)$$

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$$O_{nz} = (NaN \wedge O_1^{<3000>} + 1 \wedge O_1^{<0300>} + 2 \wedge O_1^{<0030>} + 3 \wedge O_1^{<0003>}) \quad (9)$$

The operation of the circuit is illustrated in table 5.

D	X	Y	O_1	O_z	O_{nz}
0	0	-	0	0	NaN
0	1	-	1	NaN	1
0	2	-	2	NaN	2
0	3	-	3	NaN	3
1	-	0	0	0	NaN
1	-	1	1	NaN	1
1	-	2	2	NaN	2
1	-	3	3	NaN	3

Table5. Truth table of compact detect-zero circuit

PROPOSED MODIFIED QUATERNARY DIVISION DESIGN

The quaternary division is intricacy operation and cannot implement when the zero number found in denominator because the result is undefined, so the compact detect-zero circuit provides the possibility of implemented division operation.

Conventional safe quaternary division operation is implemented without getting NaN result. It's T-gate has four incoming data transmission lines (A, B, C, D) and one selection input [15]. Proposed the compact detect zero circuit provided invalid operation exception when given a signaling NaN operand [15].

The mathematical expressions according to Fig.6 are:

$$O_1 = (0 \wedge x^{<300>} + 1 \wedge x^{<030>} + 1 \wedge x^{<003>}) \quad (9)$$

$$O_2 = (0 \wedge x^{<300>} + 0 \wedge x^{<030>} + 1 \wedge x^{<003>}) \quad (10)$$

$$O_3 = (0 \wedge x^{<300>} + 0 \wedge x^{<030>} + 0 \wedge x^{<003>}) \quad (11)$$

$$O_4 = (2 \wedge x^{<300>} + 0 \wedge x^{<030>} + 1 \wedge x^{<003>}) \quad (12)$$

$$O_5 = (3 \wedge x^{<300>} + 2 \wedge x^{<030>} + 0 \wedge x^{<003>}) \quad (13)$$

$$O_6 = (x \wedge y^{<300>} + O_1 \wedge y^{<030>} + O_2 \wedge y^{<003>}) \quad (14)$$

$$O_7 = (O_3 \wedge y^{<300>} + O_4 \wedge y^{<030>} + O_5 \wedge y^{<003>}) \quad (15)$$

The output equations of the quaternary division design can be expressed as:

the possibility to reduce the number of incoming data transmission lines to three (A, B, C) therefore, reducing the storage memory, less number of optical mirror, and less power consumption. The quaternary optical division operation has been designed with sixteen T-gates as shown in Fig.6.

Quaternary division operation is defined by two functions given in table-6 where Q stands for modulo-4 quotient and R stands for modulo-4 reminder.

The principle operation of quaternary division operation with discrete detect-zero circuit illustrate as:

CASE 1: if X=0, Y=0, set D=0 and D_1=2 then, Q=NaN, R=NaN, but if Y=<123> then change D_1=1, and Q=0, R=0.

CASE 2: if X=1, Y=0, set D=0, D_1=2 then, Q=NaN, R=NaN, but if Y=<123> change D_1=0, and Q=<100>, R=<023>.

CASE 3: if X=2, Y=0, set D=0, D_1=2 and the outputs Q=NaN, R=NaN, but if Y=<123> then, change D_1=0, Q=<212>, and R=<002>.

CASE 4: if X=3, Y=0, set D=0, D_1=2 then, Q=NaN, R=NaN, but if Y=<123> then, D_1=0, Q=<311>, and R=<010>.
This operation if the compact detect-zero circuit using for checking quaternary input X. When quaternary input Y checked, the selection input D changes to 1.

Note that NaN refer to not a number, Most operations propagate NaN without signaling exceptions, and signal the

$$Q = (O_6 \wedge D_1^{<300>} + 0 \wedge D_1^{<030>} + NaN \wedge D_1^{<003>}) \quad (16)$$

$$R = (O_7 \wedge D_1^{<300>} + NaN \wedge D_1^{<030>} + 0 \wedge D_1^{<003>}) \quad (17)$$

Table 6. Truth table of quaternary division i) quotient (Q) and ii) reminder (R)

X/Y	1	2	3
i)quotient(Q)			
1 (↕)	1	0	0
2 (●)	2	1	0
3(♦)	3	1	1
ii)Reminder(R)			
1 (↕)	0	2	3
2 (●)	0	0	2
3 (♦)	0	1	0

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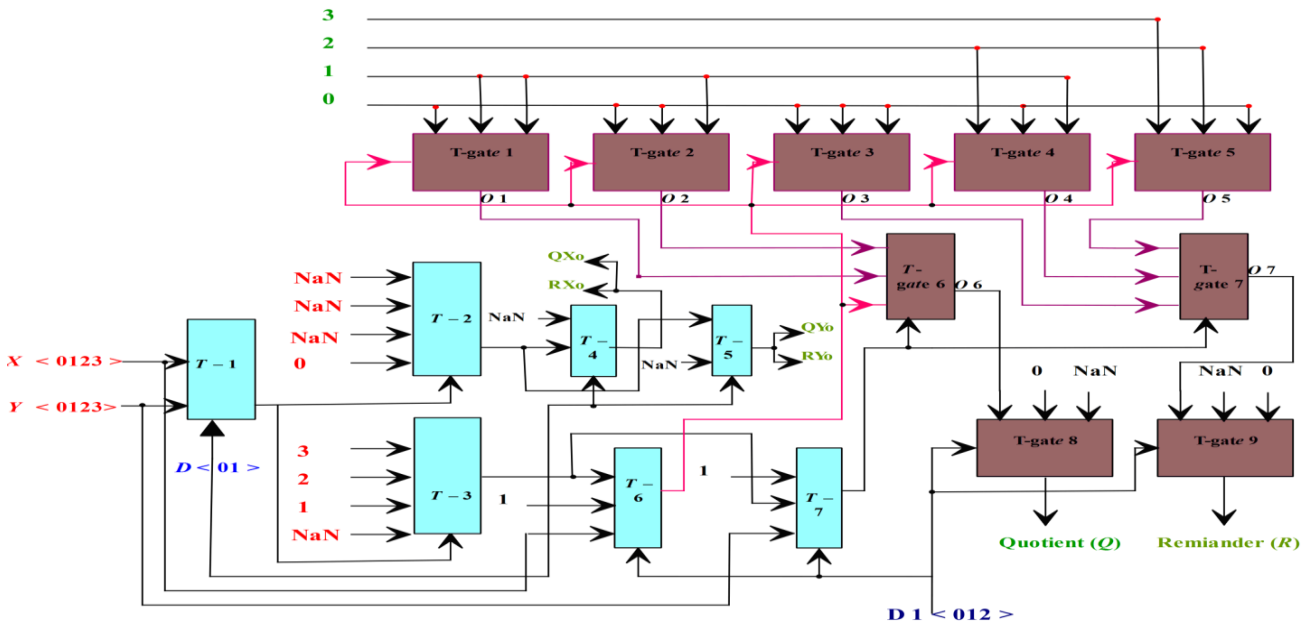
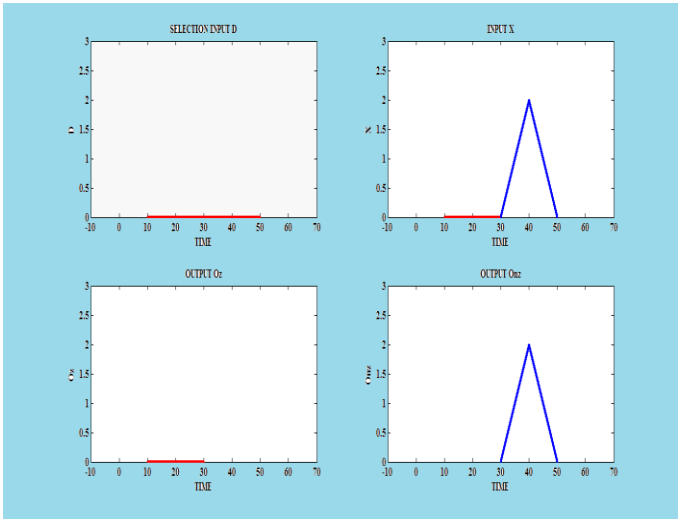


Fig.6. quaternary division operation with compact detect-zero circuit

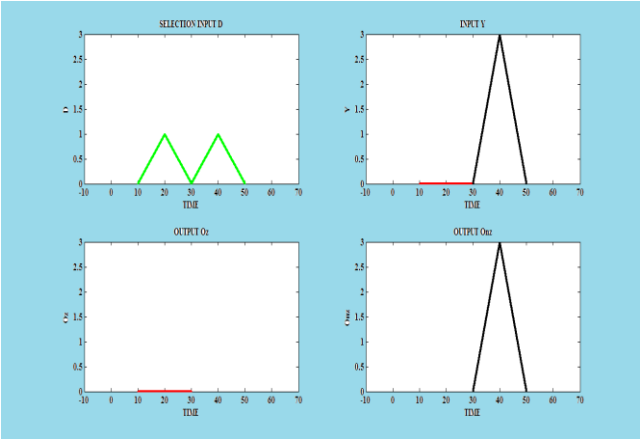
RESULT

Result of numerical simulation of TOAD based detect zero circuit with MATLAB is shown in Fig. 8. In simulation, signal X = {0, 1, 2, 3}. The pulse shape is Gaussian in nature. It is clear from the results that the output is NaN in O_{nz} if X or Y input is zero and the output O_z is equal to zero, but if input is not equal to zero then, O_z is NaN and O_{nz} is equal value of X or Y.

The compact detect-zero circuit operation depends on the selection input D. If the selection input (D) is reset to zero to check the input X whether it is equal to zero or not. Fig.8a. shows the result of the circuit into which D=0, X=<0 2>, O_z=<0 NaN>, O_{nz}=<NaN 2>. If D is set to one to check the input Y whether it is equal to zero or not. Fig.8b. shows the result of the circuit into which D=1, Y=<03>, O_z=<0 NaN>, O_{nz}=<NaN 3>.



(a)



(b)

Figure 8. Simulated waveforms of detect zero operation

D=<00>, X=<02>, O_z=<0 NaN>, O_{nz}=<NaN 2>
D=<11>, Y=<03>, O_z=<0 NaN>, O_{nz}=<NaN 3>

Figure 9 shows the simulation results of the quaternary division operation using compact detect-zero for the inputs X=<0123> and Y=<0123>. The inputs are X=<0023> and Y=<0212>, the outputs are Q=<NaN021> and R=<NaN 001>. Numerical simulation results verify the theoretical results.

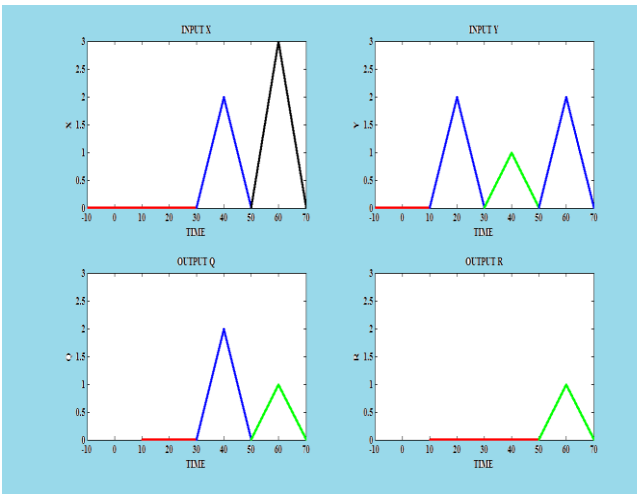


Fig9. Simulated waveforms of quaternary division operation

Conclusion and future work

A design for quaternary division operation is presented in this paper. The design is based on compact detect zero circuit. The significant advantage of this proposed scheme is that the logical operations, which can be performed, are all-optical in nature. The conventional design of T-gate used four incoming data transmission lines and one selection input but using the proposal compact detect zero design reducing number of incoming data transmission lines to three. Laser of wavelength 1552 and 1534 nm can be used as input/control signal, respectively. The design of compact detect zero circuit introduced new horizons for the basic arithmetic operation to reduce the number of T-gates and the number of incoming data transmission lines. In the design of quaternary division with discrete detect zero circuit has seventeen T-gates, five selection inputs (X, Y, C_1, C_2, C_3) ''in press'' [16] but the design of quaternary division with compact detect aero circuit has sixteen T-gates and three selection inputs (X, Y, D), then less number of incoming data transmitting lines, reducing the storage memory, less number of optical mirror, and less power consumption. For the future work the compact detect-zero circuit will used with the quaternary arithmetic operation such as addition, subtraction, and multiplication with less number of T-gates. The design of quaternary division operation with compact detect-zero can be extended to less number of optical elements by using both TOAD and T-gates.

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