International Journal of Advanced Computer Technology (IJACT)
ISSN: 2319-7900 www.ijact.org Volume IX, Issue V, October 2020

Design of Low Power and Power Scalable Pipelined ADC Using Current Modulated Power Scale

Dharmesh Kumar Pathak[1], Bakha Khambra[2]
Department of Electrical & Electronics Engineering[1]
NRI Institute of Information Science & Technology, Bhopal, MP, India
pathak.dharmesh@gmail.com[1]

Abstract: *This work represents a power scalable pipelined ADC, which achieves low power variation depends upon the sampling rate and enables variation in throughput. The keys to power scalability at high sampling rates were current modulation-based architecture and the development of novel rapid power-on Op-amp, which can completely and quickly power on/off by the feedback approach. The result achieved in this design is as high as 50 Msps and as low as 1 ksps, keeping some important parameters of ADC as ENOB and SNDR are almost constant. Power variation in ADC has a flexible range from 7.5 µW to 17 mW, which is lower power consumption than previous works.*

Keywords: Pipelined ADC, CMOS, low power, memory effect, opamp sharing, subsampling

1. Introduction

Since analog subsystems are carefully characterized and optimized by setting specific bias currents, a significant variation of bias currents reduces power with speed. Furthermore, as bias currents reduced, transistors shift from strong to weak inversion operation.

A 10-bit pipelined Analog to Digital converter (ADC) designed such that its average power is scalable with a sampling rate over a large variety of sampling rates. The ADC uses a fast power resettable Opamp (PROamp) to achieve power scalability between sampling rates as high as 50 Msps, as low as 1ksps while having 54-56 dB of SNDR all sampling rates.

Low-power analog-to-digital converters (ADCs) with 10– 12-bit resolution and several tens of MHz sampling rates are recognized as one of the significant components in portable or battery-operated commercial applications, including data communication and image signal processing systems. Recently, a lot of low-power technologies are proposed and verified in several designs. However, the time-interleaving architecture [1] easily limited by offset and gain mismatches and aperture errors between the interleaved channels.

The pseudo-differential architecture [2] compared with that of the fully differential one, is sensitive to the standard mode voltage and substrate or power supply noise. Complex calibration schemes and circuit techniques [3] are usually needed to enhance the linearity and correct the mismatches such as compensating low gain, low bandwidth, and incomplete settling of opamps, which require a complicated algorithm, additional digital circuitry, and extra calibration cycles. SHA-less and opamp-sharing are two important ways for low-power pipelined ADC design [4].

However, they also bring some drawbacks affecting the ADC performance, such as nonlinearity and distortion. How to trade off and eliminate these bad factors are the hot points in the low-power Pipelined ADC design area. Reference [5] uses dummy sampling capacitances and complicated digital calibration without opamp-sharing to enhance SNR and SFDR performance. The proposed structure in [6] may not be suitable for the ADCs that expected to run at the maximum achievable sampling rate for a given resolution and technology, Because the opamp used in the proposed first stage needs to be faster, simultaneously meaning more power consumption, than the one in the traditional first stage[7].

A current modulation technique avoids weakly inverted transistors for low bias currents, thus avoiding less accurate simulation, poorer matching, and increased bias sensitivity. The resettable power Opamp used. Simulated results show an ADC using power resettable Op-amp has 30-40% less power than an ADC, which does not use resettable power Opamp [8].

Analog-to-Digital Converters (ADC) is required for interfacing analog signals to digital circuits[9]. Sigma Delta ADC architectures are very useful for lower sampling rates and higher resolution (approximately 12-24 bits). The common applications for Sigma-delta ADC architecture are found in voice band, audio, and industrial measurements. The Successive Approximation (SAR) architecture is very suitable for data acquisition; it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 kHz to 50 MHz

2. ADC architecture

2.1 ANALOG VS DIGITAL INFORMATION

Analog signals have an infinite number of output states, whereas digital outputs have a finite number of states. Illustrations of analog and digital signals are given in Figure1 and Figure 2, respectively.

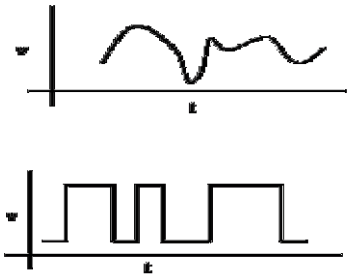


Figure 1 Example of an analog signal, Figure 2 Example of a digital binary signal

As digital signals have a finite symbol set, they can accurately recover at a receiver than analog signals. For example, suppose a white noise source distorts a transmitted binary digital signal. In that case, it is still possible to precisely determine if a '1' or '0' was transmitted so long as the noise source is sufficiently small (maximum noise limitations on digital signaling can be found in [11]). If a transmitted analog signal encounters the same noise source, however, the received analog signal is permanently distorted as shown in Figure 3; thus, the transmitted signal cannot be accurately recovered (since an analog signal can be any value between maxima, the receiver cannot accurately distinguish the noise from the signal). With modern communication systems requiring fast and accurate signaling over noisy channels (e.g., air, telephone wires, coaxial cables, power lines, etc.), digital transmission is shown in Figure 4.

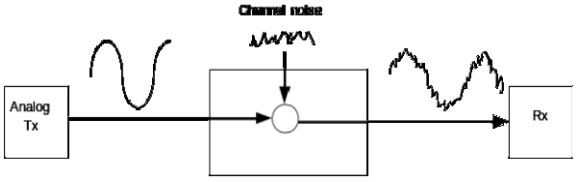


Figure 3 Analog Signal Transmission

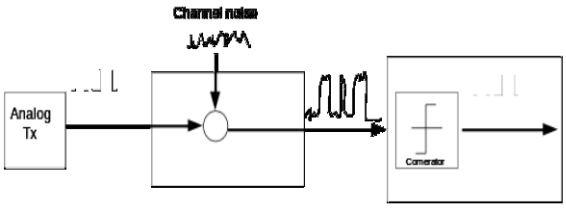


Figure 4 Digital Signal Transmission of Binary Data

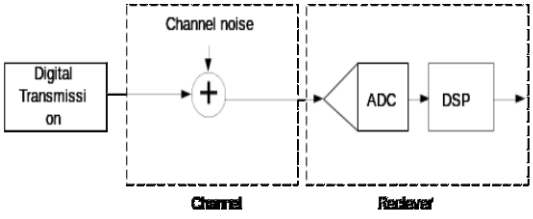


Figure 5 ADC in Signal Path of a Digital Communication System

Although digital transmissions facilitate simpler receivers, channel distortion (e.g., echo, cross-talk, skin effect losses, etc.), which cannot be removed with a single comparison operation as shown in Fig.4, necessitate more complicated receivers which perform mathematical analysis to recover the transmitted signal. As a mathematical analysis can be easily performed in the digital domain, an ADC must convert the noisy receiver input to a digital representation for digital signal processing, as shown in Fig. 5.

3. RELATED WORK

3.1 Literature Review of 10-Bit ADCS

A brief review of publication on 10-bit is presented here. As a discussion of the approaches used in each publication would be prohibitively long, this section takes note of the key performance metrics for this work, namely power, accuracy, and speed.

An increasing number of IC compatible sensors demand suitable readout circuits with on-chip ADC to reduce the signal sensitivity to perturbations on the circuit and at the sensor interface, decrease system complexity and cost, and enable further on-chip digital processing like data correction. Applications like wireless sensor nodes and medical diagnose always require at least 12-bit linearity and noise performance and extremely low power consumption (as low as 100μW) because of the battery operation. To meet large sensor arrays' requirements, the ADC must occupy a small silicon area and multiplex between multiple channels. A 100μW, 13bit ADC used for sensor array applications is presented [1].

A pipelined analog-to-digital converter (ADC) architecture suitable for high-speed (150 MHz), Nyquist-rate A/D conversion is presented. At the converter's input, two parallel track-and-hold circuits were used to separately drive the sub-ADC of a 2.8-b first pipeline stage and the input to two time-interleaved residue generation paths. Beyond the first pipeline stage, each residue path includes a cascade of two 1.5-b pipeline stages followed by a 4-b "backend" folding ADC. The full-scale residue range at the pipeline stages' output is half that of the converter input range to conserve power in the operational amplifiers used in each residue path. An experimental prototype of the proposed ADC has been integrated into a 0.18-/spl mu/m CMOS technology and operates from a 1.8-V supply. At a sampling rate of 150 MSample/s, it achieves a peak SNDR of 45.4 dB for an input frequency of 80 MHz. The power dissipation is 71 mW[2].

Article[3] describes a 10-bit 30-MS/s subsampling pipelined analog-to-digital converter (ADC) implemented in a 0.18 mum CMOS process. The ADC adopts a power-efficient amplifier sharing architecture in which additional switches are introduced to reduce the cross-talk between the two opamp-sharing successive stages. A new configuration is used in the first stage of the ADC to avoid using a dedicated sample-and-hold amplifier (SHA) circuit at the input and to avoid the matching requirement between the first multiplying digital-to-analog converter (MDAC) and flash input signal paths.

Article[4] describes a 12-bit 125-MS/s pipelined analog-to-digital converter (ADC) implemented in a 0.18 µm CMOS process. A gate-bootstrapping switch is used as the bottom-sampling switch in the first stage to enhance the sampling linearity. The prototype's measured differential and integral nonlinearities are less than 0.79 at least significant bit (LSB) and 0.86 LSB, respectively, at the full sampling rate.

Complex calibration schemes and circuit techniques [5] are usually needed to enhance the linearity and correct the mismatches such as compensating low gain, low bandwidth, and incomplete settling of opamps, which require a complicated algorithm, additional digital circuitry, and extra calibration cycles.

The residue amplifiers in high-speed pipelined analog-to-digital converters (ADCs) typically determine the converter's overall speed and power performance. We propose a mixed-signal technique that exploits incomplete settling to achieve low power residue amplification. In the first stage of a 12-bit, 75-MS/s proof-of-concept prototype, the employed open-loop residue amplifier dissipates only 2.9 mW from a 3-V supply, achieving >60% amplifier power reduction over a previously reported open-loop residue amplifier implementation and achieving >90% amplifier power reduction over a conventional opamp implementation [6].

This work covers the device and circuit aspects of low-power analog CMOS circuit design. The fundamental limits constraining the design of low-power circuits are first recalled, emphasizing the implications of supply voltage reduction. Biasing MOS transistors at very low current provide new features but require dedicated models valid in all operation regions, including weak, moderate, and strong inversion. Low-current biasing also has a strong influence on noise and matching properties. All these issues are discussed, together with the particular aspects related to passive devices and parasitic effects. The design process has to be supported by an efficient and accurate circuit simulation. To this end, the EKV compact MOST model for circuit simulation is presented [7].

A 10-b 20-Msample/s analog-to-digital converter fabricated in a 0.9- mu m CMOS technology described. The converter uses a pipelined nine-stage architecture with fully differential analog circuits. It achieves a signal-to-noise-and-distortion ratio (SNDR) of 60 dB with a full-scale sinusoidal input at 5 MHz[8].

A 10 bit 60 MS/s Low-Power Pipelined ADC with Split-Capacitor CDS Technique. The proposed pipelined ADC fabricated in a pure digital 0.18-µm CMOS process consumes 18 mW at 60 MS/s from a 1.8 V power supply, without power scalability [9].

Authors of [10] proposed a 10 bit 30-Msps sub-sampling pipelined ADC that implemented in a 0.18 m CMOS process. The ADC consumes 21.6mW from a 1.8 V power supply.

Seung-Tak Ryu et al. uses power and area-saving concepts such as operational amplifier (Op-amp) bias current reuse and capacitive level shifting for a 10-bit pipelined ADC. The prototype achieves 8.8 effective numbers of bits (ENOB) for 50 MS/s. The ADC consumes 28 mW at 1.8V [11].

Masato Yoshioka et al., given a 10 bit, 125Msps, CMOS pipelined analog to digital converter. The power consumption of this ADC is 40mW at a supply voltage of 1.8V, and SNDR is 54.2 dB[12].

Article [13] given a 10 bit, 100Msps, CMOS pipelined ADC using the time-shifted CDS technique. The power consumption of this ADC is 67mW at a supply voltage of 1.8V, and SNDR is 54 dB.

D. Miyazaki et al., the proposed design of 10 bit 30 MS/s low-power CMOS ADC described. The ADC using a pseudo-differential architecture and a capacitor cross-coupled sample-and-hold stage consumes 16 mW with a single 2V supply [14].

A 10 bit, 25Msps, CMOS pipelined ADC using a low-voltage Op-amp-reset switching technique. The power consumption of this ADC is 21mW at a supply voltage of 1.4V, and SNDR is 48 dB [15].

4. Pipeline ADC Design

As pipeline stages operate on discrete-time signals (since each step has a sample and hold), switched capacitor circuits are used for pipeline ADCs. With switch capacitor circuits, it is possible to perform highly accurate mathematical operations such as addition, subtraction, and multiplication (by a constant) due to capacitors' availability with a high degree of relative matching. Switch capacitor circuits also facilitate multiple, simultaneous signal manipulations with relatively simple architectures. It is possible to combine the functions of sample and hold, subtraction, DAC, and gain into a single switched capacitor circuit, referred to as the multiplying

digital-to-analog converter (MDAC), as shown in Figure 6.

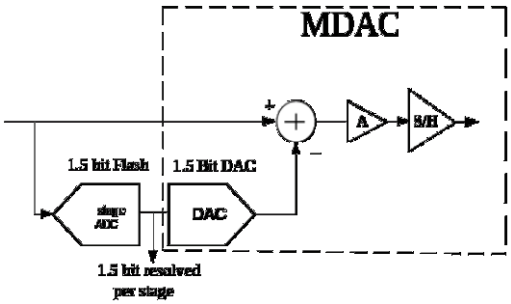


Figure 6 MDAC Functionality in dashes

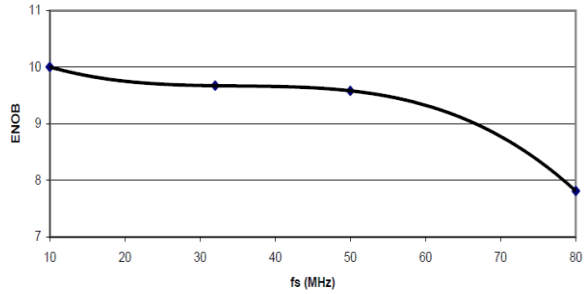
5. POWER SCALABLE AND LOW POWER ADC USING POWER RESETTABLE OP-AMPS

A scalable power range over a large range of sampling rates achieved without resorting to extensive current scaling, thus avoiding the problems of MOS transistors biased in weak inversion. A general architecture for power scalable ADCs using a Current Modulated Power Scale (CMPS) approach presented, where the application of CMPS to pipeline ADCs forms this work's focus. Methods to modulate currently presented, where a novel fast Power Resettable Op-amp (PROamp) using a replica bias approach is shown to allow for CMPS to be used at high sampling rates in pipeline ADCs.

The short on/off times of the PROamp is also shown to facilitate significant power reductions of Op-amp power in the MDACs of conventional pipeline ADCs and more generally switched capacitor circuits, which have a clock phase that does not require a virtual ground. The MDAC stages are designed to power off during the sampling phase and optionally remain on during the sampling phase. A measure of the power savings afforded by powering off the Op-amp during the sampling phase can be measured. Design choices and justifications are presented, with simulation results in SPICE given to validate the architecture.

6. SIMULATION RESULTS

The power scalable pipeline ADC with hybrid CMPS architecture was simulated at the top level using SPICE over process and temperature. This section presents a summary of key simulations and their results to provide a functional/performance verification.



Simulated ENOB for various sampling rates, while the ADC operates in power reduction mode, is shown in Figure 7 (ignoring thermal/Opamp noise and power supply noise). The ENOB was measured such that the power was scaled for each sampling rate to have minimal power for accuracy near 10-bits.

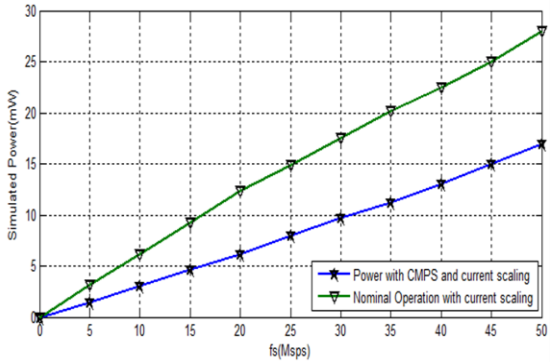


Figure 7 sampling rates of the ADC

Reduced Opamp gain for a later stage in a pipeline achieved by removing switched replica Op-amp, as shown in Fig. 8, simulation-based power of all stages (except step 9) is shown in Figure 9.

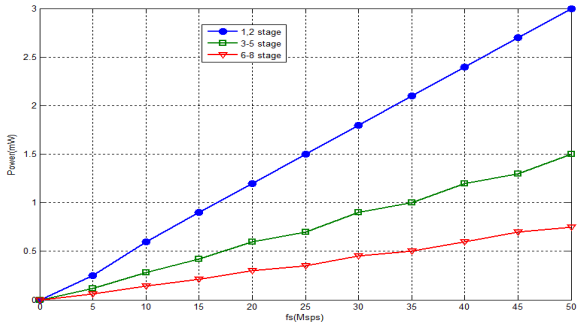


Figure 8 Opamp gain

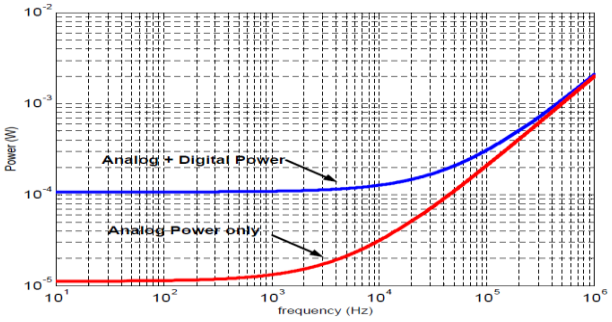


Fig.9 power of all stages

7. Conclusions

The current modulated power scale technique used previously, not been applied to ADCs faster than a few hundred ksps. As such previous power scalable ADCs were relegated to slower architectures (e.g., SAR, cyclic, etc.) due to the lack of available circuits that can power on/off in short time intervals.

The key to power scalability at high sampling rates in this work is the development of a Power Resettable Op-amp (PROamp), which by a replica bias technique, can completely and quickly switch power on/off. The application of the PROamp to a high-speed pipeline architecture in parallel with current scaling over a relatively small range (1:50) was shown to result in an ADC which had its analog power a function of frequency lower than 1ksps (7.5μW) and higher than 50Msps (17mW) while maintaining an SNDR of 54-56dB over the entire power scalable range.

References

[1]. Arias, J., Boccuzzi, V., Quintanilla, L., Enrı´quez, L., Bisbal, D., Banu, M., "Low-power pipeline ADC for Wireless LANs," IEEE Journal of Solid-State Circuits, 39(8), pp.1338–1340, 2004.

[2]. Limotyrakis, S., Kulchycki, S. D., Su, D. K., & Wooley, B. A., "A 150-MS/s 8-b 71-mW CMOS time-interleaved ADC", IEEE Journal of Solid-State Circuits, 40(5), pp.1057–1067, 2005.

[3]. Miyazaki, D., Kawahito, S., & Furuta, M., "A 10-b 30-MS/s low-power pipelined CMOS AD converter using a pseudo-differential architecture", IEEE Journal of Solid-State Circuits, 38(2), pp. 369–373, 2003.

[4]. Lee, S. C., Kim, K. D., Kwon, J. K., Kim, J., & Lee, S. H., "A 10-bit 400-MS/s 160-mW 0.13-mm CMOS dual-channel pipeline ADC without channel mismatch calibration", IEEE Journal of Solid-State Circuits, 41(7), pp.1596–1605, 2006.

[5]. Hsueh, K.-W., Chou, Y.-K., & Tu, Y.-H, "A 1 V 11b 200MS/s pipelined ADC with digital background calibration in 65 nm CMOS", ISSCC Digital Technical Papers, 30(4), pp.546–547, 2008.

[6]. Iroaga, E., & Murmann, B., "A 12-bit 75-MS/s pipelined ADC using incomplete settling. IEEE Journal of Solid-State Circuits", 42(4), pp.748–756, 2007.

[7]. Enz, "CMOS Low-power analog circuit design, Designing Low Power Digital Systems," Emerging Technologies," pp. 79-133, 1996

[8]. Lewis, S. H., Scott Fetterman, H., Gross, G. F., Ramachandran, Jr. R., & Viswanathan, T. R., "A 10-b 20-M sample/s analog-to-digital converter", IEEE Journal of Solid-State Circuits, 27(3), 351–358, 1992.

[9]. Jin-Fu Lin; Soon-Jyh Chang; Chun-Cheng Liu; Chih-Hao Huang, "A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.57, no.3, pp.163-167, March 2010

[10]. Jian Li, Xiaoyang Zeng, Lei Xie, Jun Chen, Jianyun Zhang, Yawei Guo, "A 1.8-V 22-mW 10-bit 30-MS/s Pipelined CMOS ADC for Low-Power Subsampling Applications", *IEEE Journal of Solid-State Circuits*, vol.43, no.2, pp.321-329, Feb. 2008

[11]. Ryu, S.T.; Song, B.S.; Bacrania, K., "A 10-bit 50-MS/s Pipelined ADC With Op-amp Current Reuse", *IEEE Journal of Solid-State Circuits*, vol.42, no.3, pp.475-485, March 2007

[12]. Masato Yoshioka et al, "10-bit, 125 Ms/s, 40 mW Pipelined ADC in 0.18 μm CMOS",*FUJISU Sci.J*,42,2,248-257(April 2006)

[13]. Jipeng Li; Un-Ku Moon, "A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique,", *IEEE Journal of Solid-State Circuits*, vol.39, no.9, pp. 1468- 1476, Sept. 2004

[14]. D. Miyazaki et al., "A 10-b 30-MS/s low-power pipelined CMOS A/D converter using a pseudo-differential architecture", *IEEE Journal of Solid-State Circuits*, vol 38, February 2003, pp. 369-373

[15]. D. Chang et al., "A 1.4-V 10-bit 25 MS/s pipelined ADC using Op-amp-reset switching technique", *IEEE Journal of Solid-State Circuits*, vol 38, August 2003, pp. 1401-1404

[16]. B. Hernes et al, "A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13μm Digital CMOS",*IEEE International Solid-State Circuits Conference (ISSCC)*, vol 47, February 2004, pp. 256-257.

[17]. K. Gulati et al., "A Low-Power Reconfigurable Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, vol 36, December 2001, pp. 1900-1911.