International Journal of Advanced Computer Technology (IJACT)

ISSN:2319-7900

DESIGN AND ANALYSIS Of 4BIT COUNTER USING PULSE TRIGGERED FLIP-FLOP

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Abstract

The choice of flip-flop technologies is an vital importance in design of VLSI integrated circuits for high speed and high performance CMOS circuits. In this paper, is to design a Low-Power Pulse-Triggered flip-flop which has small delay and low power consumption. First, the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Low power 8-counter is implemented using the proposed low power pulse triggered flip-flop with conditional pulse enhancement scheme.

Keywords: Flip-flop, pulse triggered and low power.

Introduction

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master– slave based FF in the applications of high-speed operations. P-FF designs can be classified as implicit or explicit. In an implicit-type P-FF, the pulse generator is a built- in logic of the latch design and no explicit pulse signals are generated. In an explicit-type PFF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse- enhancement scheme. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced [4].

Implicit Type P-FF

Ip-DCO (Implicit Pulsed-Data Close to Output)

The ip-DCO is an efficient design, is given in Fig 1(a). The pulse generator is AND based logic and a semi-dynamic structured latch design which can interface both dynamic and static structures. Implementing logic designs are easy and delay penalty is small. It occupies small area and also it uses single phase clocking. It has Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The complementary of the clock signal is taken and it is delay skewed and applied as the input to the pulse generator to generate a transparent window equal in size to the delay by inverters I1-I3. There are two disadvantages. It has larger switching power and there is a larger capacitance load which causes speed and performance degradation.

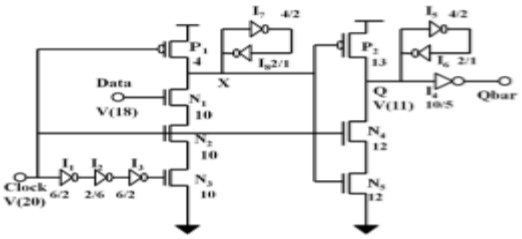

Figure 1.Circuit Diagram of IP-DCO Flip-Flop

ISSN:2319-7900

MHLFF (Modified Hybrid Latch Flip-flop)

Static latch structure is employed. Precharging of the node reduces the delay, but the power consumption is increased. Here the periodical precharging of node by the clock signal does not take place. When Q is low, the node is maintained high with the help of a weak pull-up transistor P1 which is controlled by the FF output signal Q. The unnecessary discharging problem at node is eliminated by using this design. But during the "0" to "1" transition, there is a longer Data-to-Q. This is mainly because node is not pre-discharged. The area consumption is high because we need larger transistors to enhance the discharging capability. When D=Q=1 there is extra power consumption because of the floating nodes.

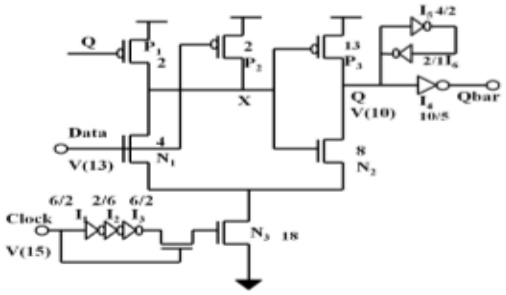

Figure 2. Circuit diagram of Modified Hybrid Latch Flip-flop

SCCER (Single Ended Conditional Capture Energy Recovery)

The first paragraph under each heading or subheading should be flush left, and subsequent paragraphs should have SCCER is a design which is a modification over the ip-DCO design. It uses a conditional discharged technique in which the discharge path is controlled by eliminating the switching activity when the input stays in stable HIGH. In this design, the back to back inverters which is used instead of pull up and pull down resistors is changed by a weak pull up transistor P1 and inverter I2 to overcome the load capacitance of node. The series connection of two nMOS transistors N1 and N2 is used in the discharge path. An extra nMOS transistor N3 is used to eliminate the unwanted switching activity. The Q_fdbk is used to control N3, so if D=1 there is no discharge. The discharge path is long when the input data is "1".

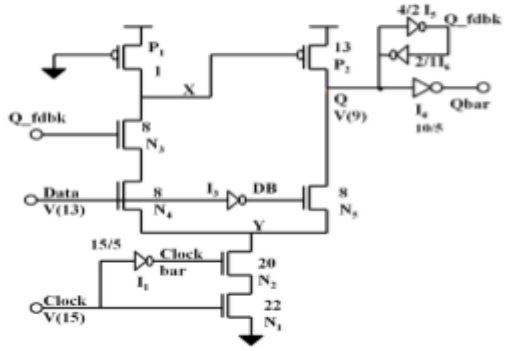

Figure 3. Circuit Diagram of SCCER Flip-flop

P-FF Design with conditional pulse

To overcome the performance degation problems of conventional P-FF the proposed model is a implicit type pulse triggered flip-flop with a conditional pulse enhancement scheme is designed. In discharging path large no. of transistors are used so more the delay and power consumption of circuit. So, in the proposed model the number of nMOS transistors in the discharging path should be reduced. There is a need to conditionally enhance the pull down strength when input data is "1". Transistor stacking design of ip-DCO in Figure 1(a) and SCCER in Figure 1(c), is exchanged by removing the transistor N2 from the discharging path. In discharging path transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1. The input to the AND logic is always complementary to each other. As a result, the output node is kept at zero most of the time. There is a floating node when both input signals equal to "0". But it doesn't provide any harm to the circuit operation. The critical condition occurs only when there is rising edges at the clock pulse. In case to pass a weak logic high to node then transistors N2 and N3 are turned ON together. This weak pulse strength is enhanced by switching ON the transistor N1 by a time cross equal to the delay provided by inverter I1. The switching power at node can be reduced due to a small voltage drop. In designed flip-flop the number of transistors in the discharging path can be reduced. The proposed p-ff speeds up the pulse generation and hence delay is reduced. The area overhead is also reduced [1].

ISSN:2319-7900

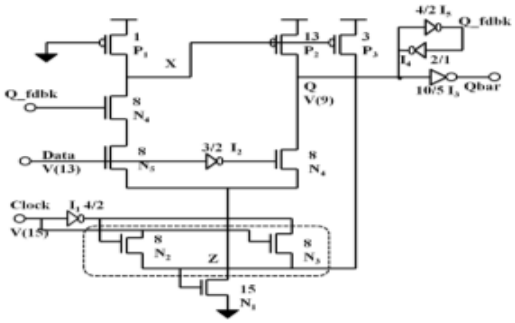

Figure 4. Circuit diagram of the P-FF design with conditional pulse enhancement scheme

SYNCHRONOUS DOWN COUNTER

The above mentioned existing pulse triggered flip-flop with conditional pulse enhancement scheme are implemented in the following synchronous down counter and the power consumption, transistor count and delay are calculated .

4bit synchronous down counter

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel).

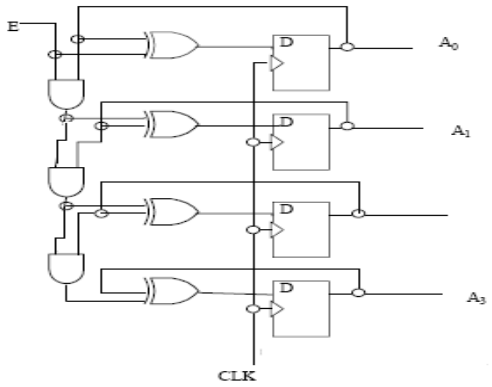

Figure 5. Circuit diagram of 4bit synchronous down counter

IMPLIMENTATION DETAILS & RESULTS

The entire work is done with the help of expansion tool TANNER EDA version 13 at 22nm technology.

Output waveforms of flip-flops

The Output waveforms of the ip-DCO and P-FF with conditional pulse enhancement scheme flip-flops are shown below the waveforms are observed over a period of 30ns. Clock and Data are inputs to the flip-flop and Q is the output of the flip-flop. It can be observed that Output follows the input for all the flip-flops.

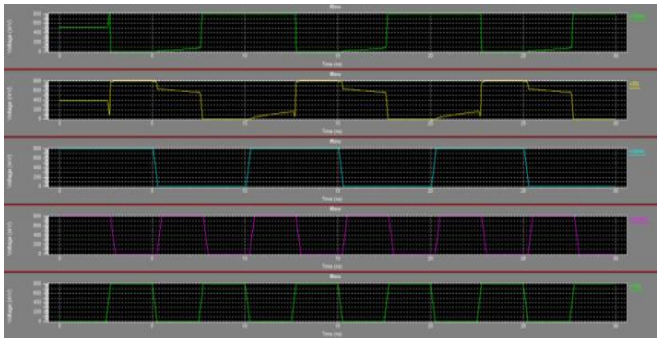

Figure 6. Simulation waveform of Ip-dco conventional pulse triggered flip-flop at 22nm

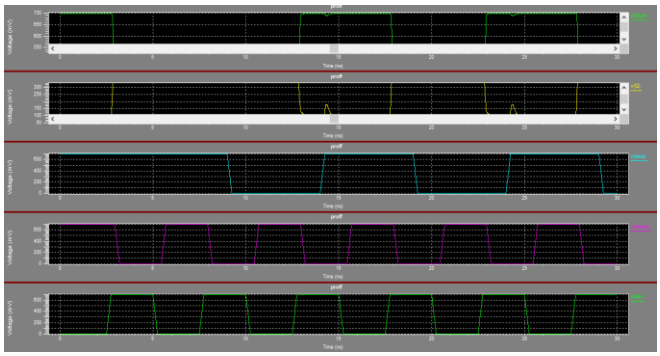

Figure 7. Simulation waveforms of Pulse flip-flop conditional enhancement scheme at 22nm.

Output waveform of 8bit synchronous down counter

The Output waveform of 8bit synchronous down counter by using P-FF with conditional pulse

enhancement scheme is shown below the waveform observed over a period of 700ns.

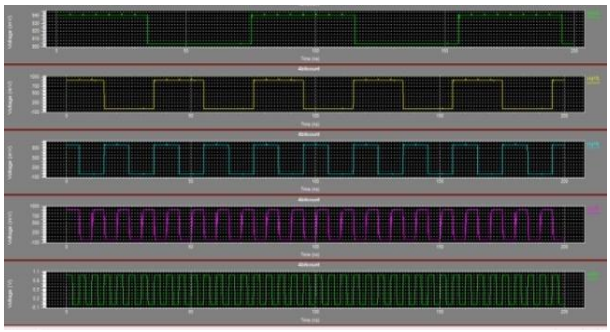

Figure 8. Simulation waveforms of 4bit synchronous down counter

Comparison chart of parameters of proposed pulse triggered flip flops between Ip-Dco and CPE work

Table 1. Power consumption of Proposed p-ffs at various technologies:

Tech.	180nm (uW)	90nm (uW)	65nm (uW)	45nm (uW)	32nm (uW)	22nm (uW)
Ip-DCO	36.8	11.4	5.9	1.5	2.4	1.7
P-FF with CPE	23.6	10.6	0.82	1.0	1.6	2.3

Table 2. Minimum Delay of Proposed P-FFs at various technologies (180, 90, 65, 45, 32, 22nm):

Tech.	180nm (ns)	90nm (ns)	65nm (ns)	45nm (ns)	32nm (ns)	22ns (ns)
Ip-DCO	0.26	0.12	2.25	0..30	2.25	5.03
P-FF with CPE	0.45	0.20	0.20	2.50	0.40	0.29

Table 3. Power-Delay-Product (PDP) of Proposed P-FFs at various technologies (180, 90, 65, 45, 32, 22nm):

Tech.	180nm (fJ)	90nm (fJ)	65nm (fJ)	45nm (fJ)	32nm (fJ)	22ns (fJ)
Ip-DCO	9.56	1.36	13.2	0.45	5.28	8.55
P-FF with CPE	10.62	2.12	0.164	2.50	0.64	0.67

Table 4. Comparison chart of parameters of 4bit Counter synchronous down Counters using CPE P-FF at 22nm technology:

	Transistors Used	Power Consumption (um)	Delay (ns)
4bit counter	116	128.8	0.89

Conclusion

To overcome the degradation performance of conventional P-FF design a proposed P-FF model which is pulse triggered flip-flop based on pulse conditional enhancement. In proposed model clock generation circuit AND function is eliminated and exchanged with PTL (Pass-Transistor Logic) based AND function. In PTL style AND function two nMOS transistors are connected in parallel and provide faster discharging of pulse. In pulse triggered flip-flop based on pulse conditional enhancement design increase the efficiency and minimize the power consumption due to reduced switching activities. The pulse triggered flip-flop based on pulse conditional enhancement scheme is used to design counters. The counters are designed using existing and proposed pulse triggered flip-flop using CMOS design with nano technology to achieve low power, less delay, and power delay product. Design of 8bit counter using TANNER EDA version 13 software tool at 22nm technology.

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ISSN:2319-7900

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