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POWER CONSUMPTION AND MEMORY AWARE VLSI ARCHITECTURE FOR MOTION ESTIMATION

K.Priyadarshini , Research Scholar, Department Of ECE, Trichy Engineering College ;
D.Jackuline Moni ,Professor,Department Of ECE,Karunya University,Coimbator

Abstract

In this paper, the Motion Estimation algorithm which is the most computationally intensive part of the encoder is determined for Single Frame (SF) and Multi Frame(MF) using MATLAB 7.9. PSNR and computation time of Single Frame and Multi Frame are determined. PSNR values achieves close performance in comparison with search techniques and computation time of Multi-form is less with Single Frame. Low power and memory aware VLSI architecture is proposed for Integer Motion Estimation in H.264/AVC. The proposed Motion Estimation unit selects suitable Sum Of Absolute Difference (SAD) design with suitable addition operations, efficiently using the concept of data reuse and power consumption which results in fast and regular flow operation. Computations and comparisons are performed using Carry Save Adder (CSA) and Carry Look Ahead Adder(CLA) for SAD operation. Proposed architecture with CLA adder circuit performs its operation with minimum memory and power consumption. The design has been implemented on the Xilinx Spartans which depicts the characteristics of memory used , and minimum power consumption for SAD unit.

Key Words: Motion Estimation, Carry Save Adder (CSA), Carry Look Ahead adder (CLA), SAD Hardware Architecture.

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Introduction

Motion estimation and motion compensation are the predictive techniques for exploiting the temporal redundancy between successive frames of video sequence. For encoding , Block matching motion estimation takes a maximum part of the processing time. An MPEG video, is represented as a sequence of frames and the small differences existing between the frames are realized by the rocess of motion vector. This best motion vector is obtained by full search block matching algorithm and various fast searching algorithms. Full search block matching algorithm provides the optimal solution by exhaustively comparing each (NXN) block of thecurrent frame with all the candidate blocks of $(N+2p)^2$ search window. In video coding system, Motion estimation (ME) plays a key role to improve coding efficiency by reducing temporal redundancy within video sequence. ME takes more than 50% computational complexity in H.264/MPEG-4 AVC [1] which is the state-of-the-art video compression standard. Block matching algorithm, which is ME algorithm used in H.264/MPEG-4 AVC, is based on dividing a frame into MacroBlocks (MBs)(16x16 pixels), and searches for the best matching block with ME process requires very high computational complexity, and it has been implemented as a dedicated hardware with reduced memory area and low power consumption. Several search techniques like Full Search [2] Fast Full Search[3] and Fast Search are present. Full search algorithm matches all possible candidates with a minimal distortion to find the displacement. ME refines the best candidate for each sub blocks using two stages Integer Motion Estimation and Fractional Motion Estimation .[4] During the first stage 41 motion vectors are determined using various searches. In IME, to determine the Motion Vector(MV), the integer pixel searches the best matching integer position using performance cost metric Sum of Absolute Difference (SAD), Mean Square Error (MSE) and Mean Absolute Difference (MAD) which gives a numerical data about how similar two blocks are.

MAD cost function's simplicity and ease of implementation in hardware tends to overemphasize small differences giving an inferior result to MSE. In algorithms [4] [5] center position of next searching step is not known until the minimum search step is
found which leads critical issues in latency and pipelining cycles. [6] Full search motion estimation algorithms follow a regular search pattern and usually provides superior visual quality in terms of PSNR compared to other motion estimation algorithms. [7] PSNR measures the difference between two images and gives a result in a figure of decibels. Higher

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values of PSNR results in small differences between two images [8].

In this paper, motion vectors for a single reference frame and multiframes are determined for sample sequences and a comparative analysis is done based on PSNR value and computation time for the cost metrics MSE .The rest of the paper is organized as follows: Section 2 deals with the search techniques and features of PSNR values of multi frame motion estimation. Section 3 deals with the architecture design of SAD using CSA and CLA. Section 4 figures out the simulation results with the comparison chart. Section 5 concludes the paper.

SEARCH TECHNIQUES

Fast block matching algorithms Full Search (FS),Three Step Search(TSS), New Three Step Search (NTSS), Four Step Search(FSS,) Diamond Search (DS) reduces up the number of computations by decreasing the number of search points which leads to poor PSNR computations

FRAME MOTION ESTIMATION

1. PSNR value of Single Frame and Multi Frame Processing for various video sequences using MSE

Video Sequence	PSNR Value									
	Full Search (FS)		Three Step Search (TSS)		New Three Step Search (NTSS)		Four Step Search(FSS)		Diamond Search (DS)	
	Single Frame	Multi Frame	Single Frame	Multi Frame	Single Frame	Multi Frame	Single Frame	Multi Frame	Single Frame	Multi Frame
Akiyo_ QCIF(518X350)@15 fps [2x2]	34.18	31.38	31.72	29.65	26.90	22.44	33.46	31.40	32.94	30.93
Car (320x240)@50fps[2x2]	23.8	19.97	20.9	17.9	17.3	15.45	26.6	22.4	23.51	23.51
Vipmen (160X120)@100fps[2x2]	27.80	21.62	26.12	21.69	22.92	18.50	31.18	27.51	27.75	23.8

Table 2. Computation Time of Single Frame and Multi Frame Processing for various video sequences using MSE

Video Sequence	COMPUTATION TIME									
	Full Search (FS)		Three Step Search (TSS)		New Three Step Search (NTSS)		Four Step Search (FSS)		Diamond Search (DS)	
	Single Frame	Multi Frame	Single Frame	Multi Frame	Single Frame	Multi Frame	Single Frame	Multi Frame	Single Frame	Multi Frame
Akiyo_ QCIF(518X350)@15 fps [2x2]	87.71	86.6	37.22	38.96	70.02	63.08	101.89	98.46	67.68	62.36
Car (320x240)@50fps[2x2]	122.0	120.03	50.57	50.06	90.3	88.9	113.58	122.86	178.3	173.8
Vipmen (160X120)@100fps [2x2]	30.93	28.67	13.6	13.5	22.21	22	24.02	25.41	37.37	37.00

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ARCHITECTURE DESIGN

The main characteristic of the proposed architecture is the large amount of Processing Element Units (PE's) that are used to calculate SAD (Sum Of Absolute Difference)metric.

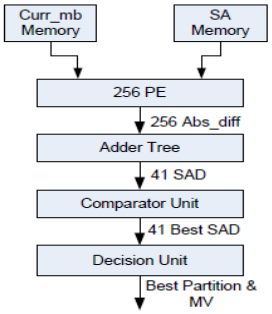

Figure 2 Motion vector determination unit

Fig.2 shows the Motion vector determination unit which consists of Search Area (SA) memory, a processing array which contains 256 Processing Elements, Adder Tree, comparator and Decision unit. The data in the memory are stored in a ladder like manner to avoid delay. The 256 absolute differences are summed up by the adder tree and the outputs are the 41 block partitions. [10] Two types of adders CSA and CLA are processed and compared. The comparator updates the minimum SAD throughout the scanning process for the 41 block partition.

SAD UNIT

The sum of absolute differences (SAD) algorithm determines if two blocks of data are identical. Blocks tend to be either an 8x8 block or 16x16 block of 8-bit pixels. When the sum of the absolute differences between the respective pixels in two blocks is zero, the blocks can be considered identical and a motion vector is calculated . Using motion vectors we can significantly reduce the number of pixels transmitted per frame. [8] The internal structures of the PE is composed by a large number of addition to calculate the SAD's. Fig 3 shows that the SAD block computes SAD between current and reference blocks and passes that value to the comparator. The comparator compares the SAD value with a threshold value and gives the result to the motion estimation block. Threshold value is chosen randomly and it depends on the type of application. If the SAD is less than the threshold value, we assign zero motion vectors for that block. If the SAD value is greater than the threshold value then the motion estimation block finds the motion vectors for operation is very time consuming due to the complex nature of the absolute operation. All the absolute operations of the SAD operation are performed serially, per column in parallel, per row in parallel, operations in parallel .

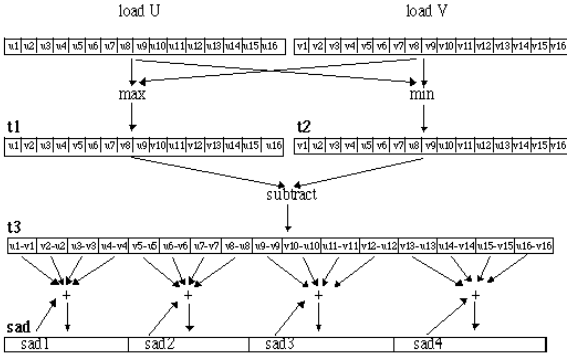

Figure 3.Calculation Of Sum Of Absolute Difference

The proposed PE Units are proposed to calculate the SAD with reduced computation complexity and delay. The ME unit requires 256 clock cycles for each MB search. [12] [13]The input and output for the adder tress is 8 bits wide and the SAD output is 4 and 16 bits wide. These data are then input into the comparator , together with the current search location information. These data are then input into the comparator, together with the current search location information.

ADDER UNIT

The Carry Look Ahead [11] improves speed by reducing the amount of time required to determine carry bits. Carry Look Ahead logic uses the concepts
of generating (G) and propagating (P) carries. The Carry-Look Ahead adder is broken up in two modules. Carry-Save Adders (CSA) is useful in situations when we need to add more than two numbers, since this design automatically avoids the delay in the carry–out bits. The proposed architecture is designed with CLA and CSA.

SIMULATION RESULTS

Table III reports the synthesis details of the proposed architecture.

S.No	Parameter	Adder Unit		Motion Estimation Unit		
		CSA (8 bit)	Proposed CLA (16 bit)	SAD Unit (8 bit)	Comparator Unit (8 bit)	Decision Unit (8 bit)
1.	Path Delay	21.831 ns	6.261 ns	6.236 ns	8.61 ns	6.546 ns
2.	Memory Usage	185300 KB	156236 KB	160404 KB	160404 KB	160404 KB
3 .	Power Consumption	247 mw	227 mw	262 mw	167 mw	211 mw

5. CONCLUSION

In this paper an important coding tool of H.264 is the Motion Estimation matching algorithm. The motion estimation process from the current frame and the reference frame is simulated using Matlab software. The SAD architecture with the Adder units is implemented using Xilinx Spartan 3E FPGA. Five different algorithms for motion estimation are simulated and PSNR values are determined. It is concluded that PSNR value of multiframe processing gives minimum degradation when compared with Single frame but with decrease in processing time. Proposed architecture with CLA adder circuit performs its operation with minimum memory and power consumption.

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PRIYADARSHINI, received her B.E. degree in Electronics &Communication Engineering from V.L.B Janakiammal College of Engineering, from Bhararthiyar University, Coimbatore and M.E (Communication Systems) from Anna University, Chennai .Currently she is working as faculty in Elec-

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tronics &Communication Engineering Department in Trichy Engineering College,Trichy. She is carrying out her research work in the Department of Electronics and Communication Engineering, Karunya University Coimbatore, Tamilnadu.

Dr.D.Jackuline Moni completed her B.Tech in Electronics Engineering from Madras Institute Of Technology , Anna University , M.E from Government College Of Technology, Coimbatore and her Ph.D (VLSI Design) from Anna University, Chennai. She has published more than 40 papers in National and International Journals and conferences. She received her Ph.D from Anna University in the area of VLSI design.